ABLE
DH/DM
PRELIMINARY
USER's GUIDE

10104X07

September, 1982

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CONTENTS

Figures

Tables

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SECTION 1
HOW TO USE THIS MANUAL

Congratulations on your purchase of a DH/DM from ABLE COMPUTER. We are sure it will provide you with years of satisfactory service. We have prepared this manual to help you maximize the effectiveness of the DH/DM in your system.

This manual is provided to assist you with the installation, use and care of DH/DM; it does not provide repair information. If you have problems with your DH/DM, we prefer that you let us repair it in our factory.

This manual assumes that you are familiar with the PDP-11 architecture and Unibus structure. For information about the PDP-11, refer to the following DEC documents:

- PDP-11 Processor Handbook
- PDP-11 Peripherals Handbook
- PDP-11 Terminals and Communications Handbook

This manual is organized into the following sections:

- Section 2 provides a general description of DH/DM and lists its special features. It also includes programmable line parameter information, electrical specifications, and physical specifcations. Photographs of the DH/DM are included in this section.
- Section 3 gives a brief installation procedure, followed by detailed instructions on installation. It describes the functions of all switches on the board and tells how to set them -- address selection, vector selection, baud rate, and miscellaneous functions contained on switch S4. It provides information on maintenance features, including the microdiagnostics. This section includes information on how to prepare the system for installation, install the DH/DM, run the diagnostics, and verify installation.
- Section 4 contains information on the care of DH/DM and troubleshooting tips in the event that a problem occurs. It also tells who to contact and how to contact them for service.
- Section 5 describes a typical application for DH/DM. It provides terminal/communications information, wiring information for modem connection, and Unibus connector information.

- Section 6 contains descriptions of data handling registers, modem registers, timing considerations for transmitter/receiver speed programming, break control, and transmitter and receiver timing. It also includes maintenance mode considerations.

- Appendix A provides an interrupt level strapping chart to alter the priority level of DH/DM.

- Appendix B supplies a DH/DM list of materials.

- Appendix C contains a spare parts listing for those wishing to maintain a spare parts inventory.

SECTION 2
WHAT IS DH/DM ?

2.1 GENERAL DESCRIPTION

The DH/DM is a microprocessor-based controller which connects a Unibus system to 16 asynchronous communications lines. It provides DMA (direct memory access) output capabilities and modem control. It is system software compatible with the DEC DH11 and DM11-BB.

A basic DH/DM consists of a hex-width board, EIA distribution panel, and interconnecting cables. The DH/DM can be installed in any standard DEC DD11 peripheral mounting panel. See Figures 2-1, 2-2, and 2-3.

2.2 FEATURES

- The DH/DM requires only one hex slot rather than the dedicated nine-slot backplane used by the DH11.
- The DMA output capability frees the processor from transmit-character request interrupt handling.
- By accessing words rather than bytes, the DH/DM provides double the DH11 data transfer rate capability and cuts Unibus time in half.
- On-board clock provides a non-standard baud rate source eliminating a possible requirement for a separate clock card.
- Isolation from terminals in loopback maintenance mode eliminates unwanted printouts.
- Supports all standard DH11 baud rates, plus 19.2K baud.
- Diagnostic loopback connectors are built-in to provide ease of use.
- On-board address and vector selection switches eliminate the need for jumpers and add flexibility.

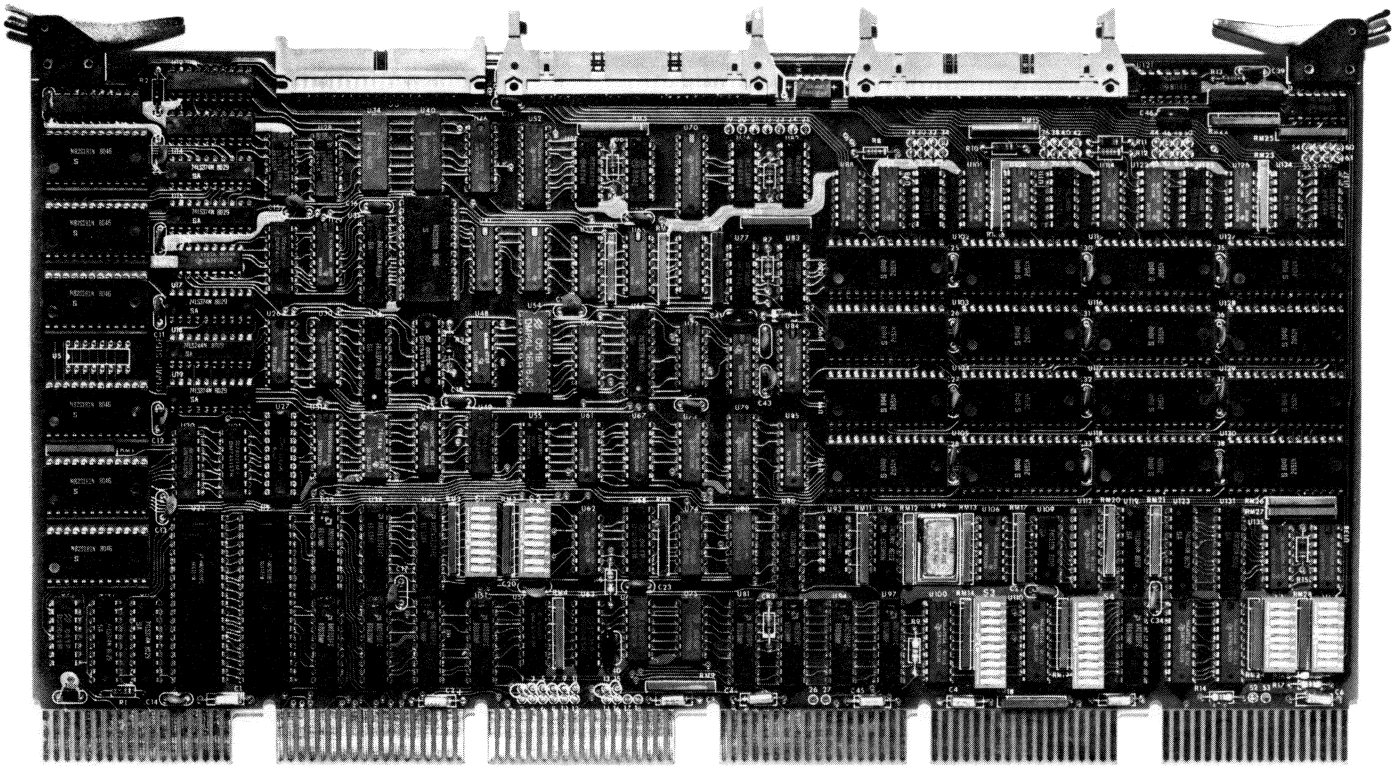

Figure 2-1: DH/DM PC Board Model 10103-1

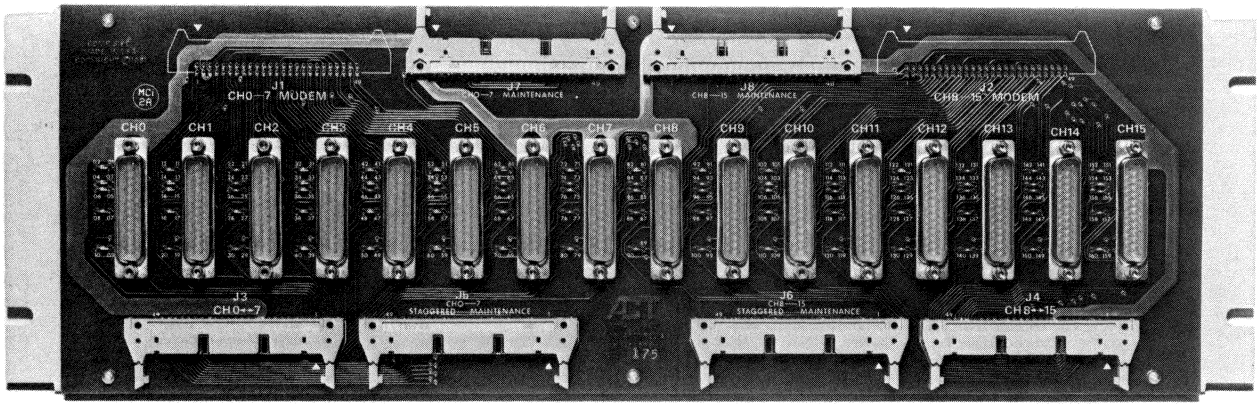

Figure 2-2: DH/DM EIA Distribution Panel

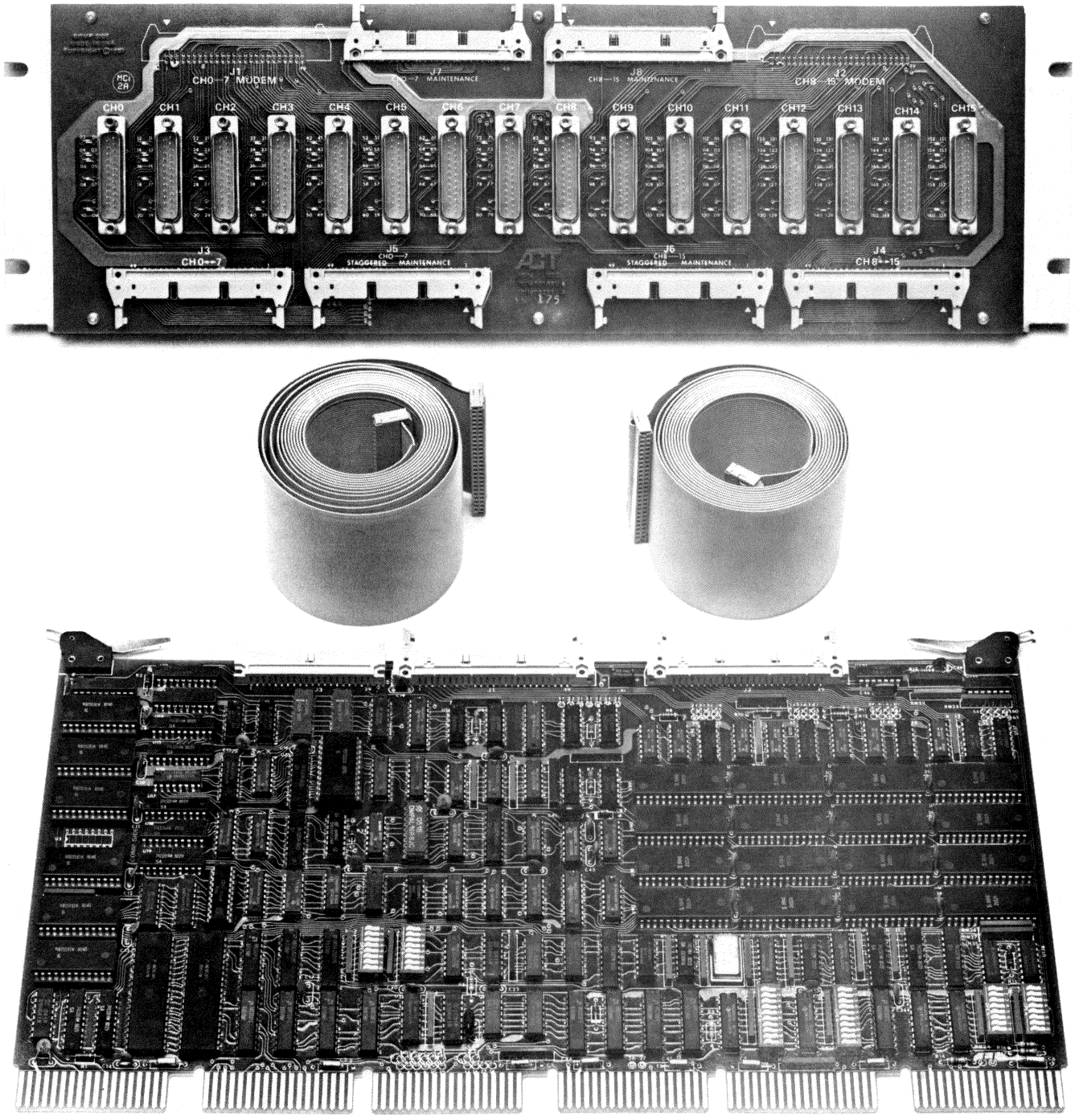

Figure 2-3: DH/DM System
Model 10100-1

2.3 SPECIFICATIONS

2.3.1 PROGRAMMABLE LINE PARAMETERS

Character Length: 5, 6, 7, or 8 data bits

Number of Stop Bits: 1 or 2 for 6-, 7-, or 8-bit characters;
1 or 1.5 for 5-bit characters

Parity Generation/Detection: Odd, even, or none

Operating Modes: Full duplex

Transmitter/Receiver Speeds (Baud): 0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19.2K, On-board external clock

2.3.2 ELECTRICAL SPECIFICATIONS

Bus Loading: The DH/DM presents one unit load to the Unibus.

Power Requirements: 4.4 amps @ + 5V
0.2 amps @ +15V
0.2 amps @ -15V

Bus Request Level: Individually selectable for receive, transmit, and modem control at levels BR4, BR5, BR6, or BR7.

Device Addresses: The DH/DM requires eight consecutive word addresses in the floating address space which starts at 760010. All DH/DM units in a system should have consecutive word addresses.

The modem control requires two consecutive word addresses, the first of which must be a multiple of four. Floating address space has been assigned for 16 boards. The first is at 770500; the second starts at 770510, and so forth.

Interrupt Vectors: DH/DM requires three consecutive interrupt vectors, XX0 for the receiver, XX4 for the transmitter, and XXX for the modem. These are in the floating vector space (000 - 774).

2.3.3 PHYSICAL SPECIFICATIONS

Board Size:	The DH/DM is a standard hex-width board. Rectangular dimensions are 15.69 X 8.4 inches. The board is shown in Figure 2-1.
Distribution Panel:	6½ x 19 inches. Uses a standard mounting to the rear RETMA rails of the computer cabinet. The EIA panel is shown in Figure 2-2.

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SECTION 3
HOW TO INSTALL DH/DM

3.1 INSTALLATION PROCEDURE

Section 3 provides a detailed description of the procedure to follow when installing a DH/DM. Below is a brief step-by-step description of the entire installation procedure.

1. Determine the address assignment of the DH portion and set switch S2 accordingly (Section 3.5 and Section 3.6.1).

2. Determine the address assignment of the DM portion and set switch S1 accordingly (Section 3.5 and Section 3.6.2).

3. Determine the vector assignment of the DH portion and set switch S5 accordingly (Section 3.5 and Section 3.6.3).

4. Determine the vector assignment of the DM portion and set switch S6 accordingly (Section 3.5 and Section 3.6.4).

5. Select the desired external B baud rate and set the switches (Section 3.7.1)

6. Refer to Table 3-9 for switch S4 functions and set switch accordingly (Section 3.7.2).

7. Set maintenance switches to achieve the desired functions (Section 3.8.1).

8. If interrupt levels other than the ones factory set are required, modify the jumper connections (Section 3.9).

9. Remove power from the system (Section 3.10).

10. Locate a vacant hex slot. If using a DEC backplane, modify it for DH/DM by removing the wire between pins CA1 and CB1 of the slot (Section 3.10).

11. Install DH/DM board in vacant slot (Section 3.11.1).

12. Install the EIA panel (Section 3.11.2).

13. Install the cables (Section 3.11.3).

14. Apply power to the system, checking the LEDs to verify internal operation of the board (Section 3.13).

15. Install EIA panel cables into maintenance connectors and run diagnostics (Section 3.13).

3.2 UNPACKING THE DH/DM

The DH/DM is shipped in special containers to prevent damage during shipment. It is recommended that these containers be saved for use in the event that the product requires subsequent reshipment. Unpack the contents carefully and inspect for any signs of damage. If damage is found, notify the carrier immediately.

3.3 VERIFY THAT YOU RECEIVED WHAT YOU ORDERED

Be sure that you received what you ordered by checking the board, panel, and cable numbers. The board number is 10103 and is found on the back side of the board in the upper right corner. The EIA panel is numbered 10114. The cables are numbered 90000186. See Figure 2-1, 2-2, and 2-3.

3.4 EQUIPMENT NEEDED TO USE THE DH/DM

You will need the following equipment to use the DH/DM:

- PDP-11 Unibus computer system
- One vacant hex SPC slot for mounting the DH/DM
- Panel mounting space (6 inches high) for the distribution panel
- One to 16 terminal devices with appropriate modems or null modems and interconnecting cables.

3.5 HOW TO DETERMINE ADDRESS AND VECTOR ASSIGNMENTS

The DH portion of the DH/DM uses eight words of floating address space. The floating address space begins at 760010 as shown in Figure 3-2. Addresses within this space are assigned according to rank. Table 3-1 shows the ranks assigned to devices addressed in this range.

The DH uses addresses located after any DJ11's in the system. Each DH requires eight consecutive addresses starting with an address that is a multiple of 20 (octal). For example, for a system with no DJ11 units, register address assignments for three DH/DM units would be as follows:

Unit	Octal Register Addresses
1st DH/DM	760020 - 760036
2nd DH/DM	760040 - 760056
3rd DH/DM	760060 - 760076

NOTE:
For special VAX/VMS driver switch settings, see Appendix D.

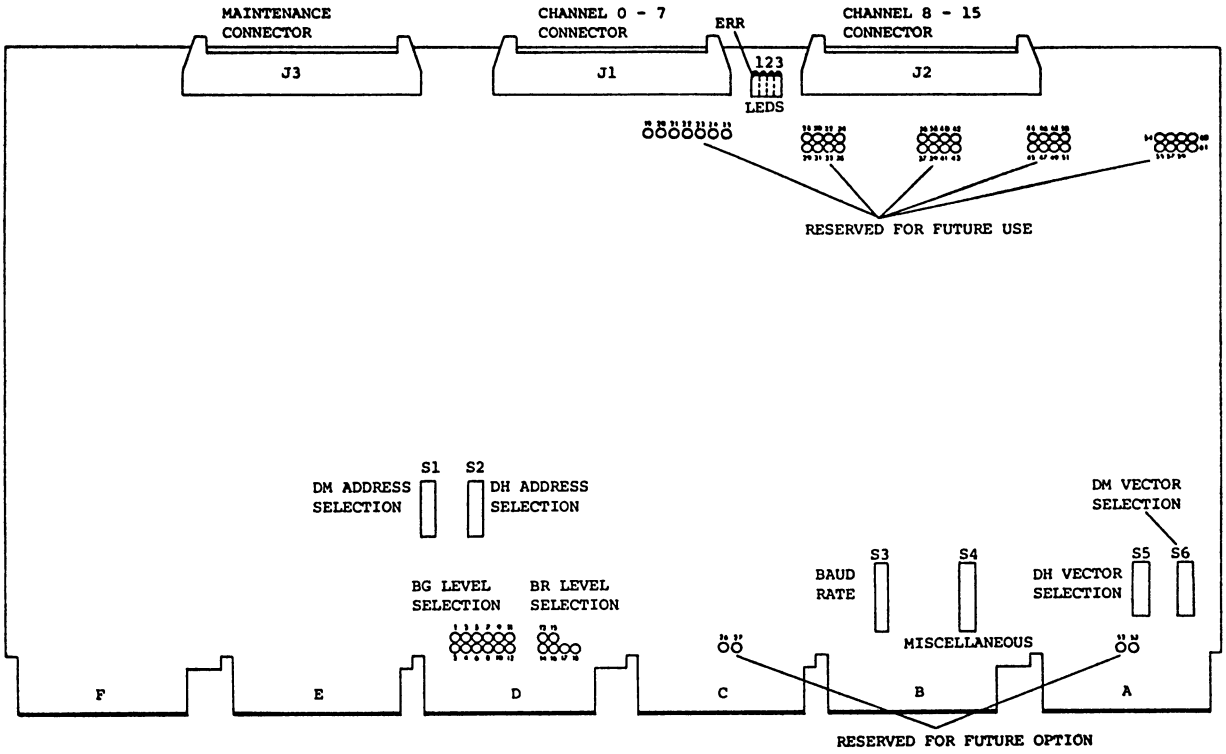

Figure 3-1: DH/DM Board Layout

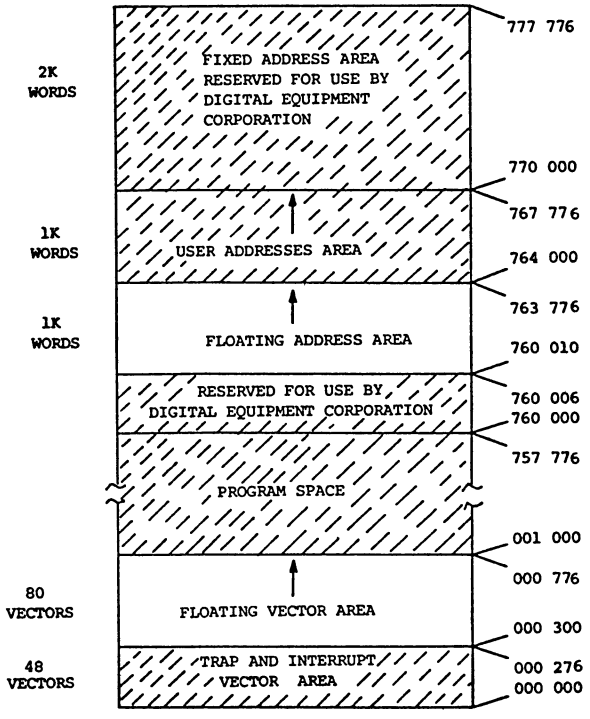

Figure 3-2: Address Map

Notice that, although the system in this example contains no DJ11 units, address 760010 cannot be assigned to the first DH/DM unit because it is not a multiple of 20 (octal).

Rank	Unibus Device
1	DJ11
2	DH11
2	DH/DM
3	DQ11
4	DU11
5	DPU11
6	LK11A
7	DMC11
8	DZ11
9	KMC11
10	RL11 (extra)

Table 3-1: Device Ranks for Floating Address Assignment

The DM portion of the DH/DM requires two additional consecutive word addresses. The addresses assigned to the registers of the first DM in a system are 770500 and 770502. The addresses for additional DM registers start at consecutive addresses which are multiples of 10 (octal). Thus, the addresses for a second DM are 770510 and 770512; those for a third DM/16 board are 770520 and 770522; and so on.

The DH uses two interrupt vectors (for the receiver and transmitter interrupts). The DM uses one interrupt vector. Vector addresses for all devices are assigned in order from 300 through 774 according to the DEC rankings listed in Table 3-2. Find the device in your system with the lowest rank number and assign this 320, etc. Next find the device with the second lowest rank number and assign it the next consecutive vector address. Continue until all vector addresses are assigned. If a device is added to an existing system, its vector address must be inserted at the normal position and all other device addresses incremented accordingly. Table 3-3 shows the sample vector addresses for the DH/DM.

RANK NUMBER	DEVICE TYPE	NUMBER OF VECTORS
1	DC11	2
2	KL11, DL11-A, DL11-B	2
2	QUADRASYNC/B	8
3	DP11	2
4	DM11-A	2
5	QUADRACALL, DN11	1
6	DM11-BB for DH11	1
6	DM portion of DH/DM	1
7	DR11-A	2
8	DR11-C	2
8	DUAL I/O	4
9	PA611 Reader	1
10	PA611 Punch	1
11	LPD11	2
12	DT11	2
13	DX11	2
14	DL11-C, DL11-D, DL11-E	2
14	QUADRASYNC/C	8
14	QUADRASYNC/E	8
15	DJ11	2
16	DH11, DMAX/16	2
16	DH/DM	2
17	GT40	4
18	LPS11	6
19	DQLL	2
20	DW11-W	2
21	DU11	2
22	DUP11	2
23	DV11	2
23	DV/16, 8 or 16 channels	2
23	DV/16, 24 or 32 channels	4
24	DV11 Modem	1
24	DV/16 Modem	1
25	LK11-A	2
26	DWUN	2
27	DMC11	2
28	DZ11	2
28	DZ/16	2
29	KMC11	2
30	LLP11	2
31	VMV21	2
32	VMV31	2
34	DWR70	2
35	RL11/RL211	1
36	RX211	1
37	TS11	1
38	LPA11-K	2
39	IP11/IP300	1
40	KW11-C	2
41	RX11	1
42	DR11-B	1

Table 3-2: Floating Interrupt Vector Devices

Device	Channels	Vector	
1st DH	0 - 15	Receiver	400
		Transmitter	404
2nd DH	0 - 15	Receiver	420
		Transmitter	424
1st DM	0 - 15		440
2nd DM	0 - 15		444

Table 3-3: Typical Vector Addresses

3.6 HOW TO SET THE DEVICE ADDRESS AND VECTOR SELECTION SWITCHES

3.6.1 DH DEVICE ADDRESS SWITCH (S2)

Device addresses for the DH portion of the DH/DM are set using switch S2. Refer to Figure 3-1 for the location of switch S2 and Figure 3-3 for switch descriptions. Use Table 3-4 to determine the device address switch settings. The starting address can be determined by referring to the information in Section 3.5.

NOTE: An open switch is accomplished by pressing the side of the switch marked "OPEN."

3.6.2 DM DEVICE ADDRESS SWITCH (S1)

Device addresses for the DM portion of the DH/DM are set using switch S1 on the board. Refer to Figure 3-1 for the location of switch S1 and Figure 3-3 for switch descriptions. Use Table 3-5 to determine the device address switch settings. The starting address can be determined by referring to the information in Section 3.5.

3.6.3 DH VECTOR ADDRESS SWITCH (S5)

Vector addresses for the DH portion of the DH/DM are set using switch S5 on the board. Refer to Figure 3-1 for the location of switch S5 and Figure 3-3 for switch descriptions. Use Table 3-6 to determine the vector address switch settings. To determine the desired vector addresses refer to Section 3.5.

3.6.4 DH VECTOR ADDRESS SWITCH (S6)

Vector addresses for the DM portion of the DH/DM are set using switch S6. Refer to Figure 3-1 for the location of switch S6 on the board and Figure 3-3 for switch descriptions. Use Table 3-7 to determine the vector address switch settings. Section 3.5 describes how to determine the desired vector addresses.

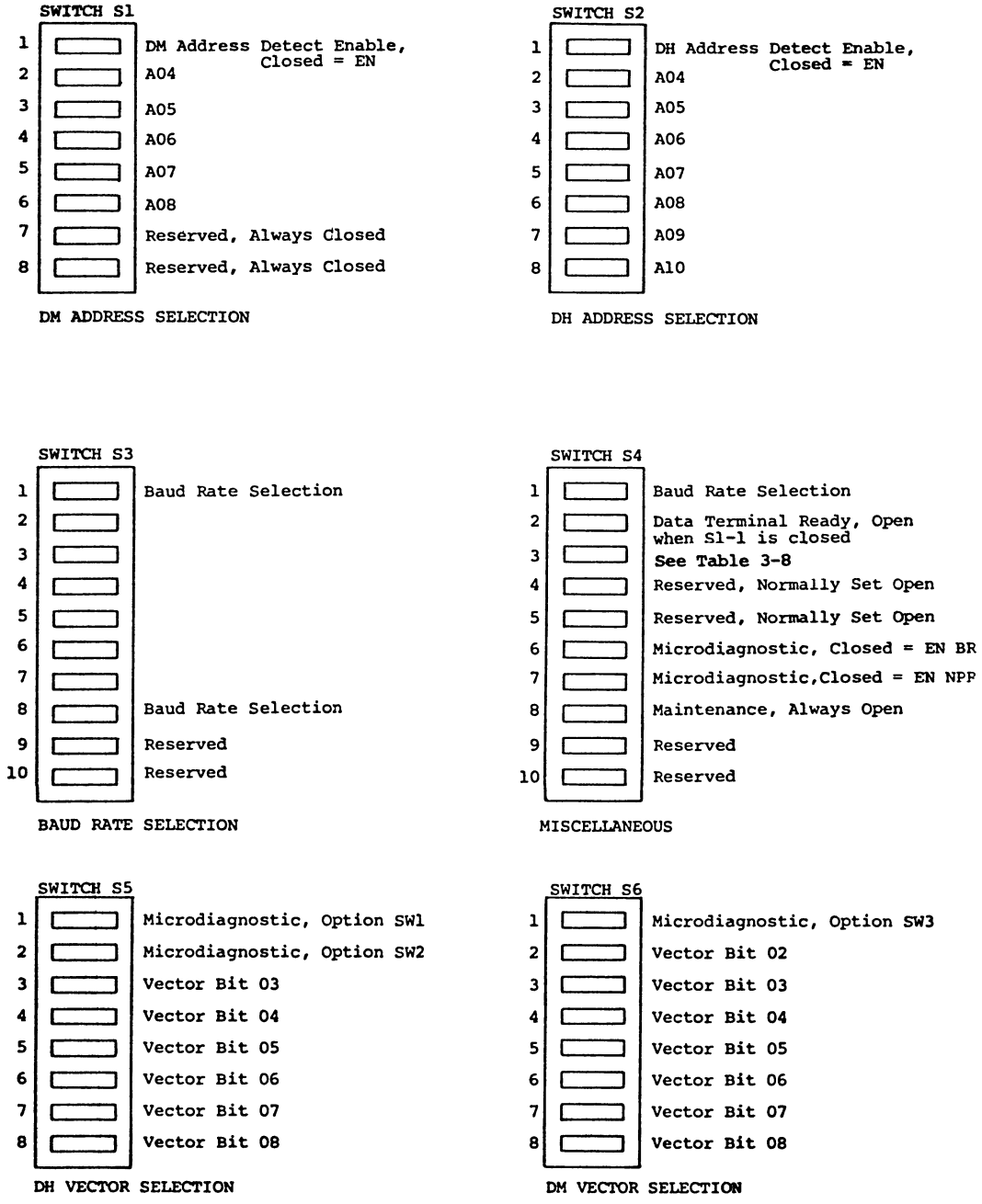

Figure 3-3: DH/DM Switch Descriptions

DH STARTING ADDRESS	SWITCH 2 POSITION								DH STARTING ADDRESS	SWITCH 2 POSITION							
	8	7	6	5	4	3	2	1		8	7	6	5	4	3	2	1
760020	C	C	C	C	C	C	-	C	761360	C	-	C	-	-	-	-	C
760040	C	C	C	C	C	-	C	C	761400	C	-	-	C	C	C	C	C
760060	C	C	C	C	C	-	-	C	761420	C	-	-	C	C	C	-	C
760100	C	C	C	C	-	C	C	C	761440	C	-	-	C	C	-	C	C
760120	C	C	C	C	-	C	-	C	761460	C	-	-	C	C	-	-	C
760140	C	C	C	C	-	-	C	C	761500	C	-	-	C	-	C	C	C
760160	C	C	C	C	-	-	-	C	761520	C	-	-	C	-	C	-	C
760200	C	C	C	-	C	C	C	C	761540	C	-	-	C	-	-	C	C
760220	C	C	C	-	C	C	-	C	761560	C	-	-	C	-	-	-	C
760240	C	C	C	-	C	-	C	C	761600	C	-	-	-	C	C	C	C
760260	C	C	C	-	C	-	-	C	761620	C	-	-	-	C	C	-	C
760300	C	C	C	-	-	C	C	C	761640	C	-	-	-	C	-	C	C
760320	C	C	C	-	-	C	-	C	761660	C	-	-	-	C	-	-	C
760340	C	C	C	-	-	-	C	C	761700	C	-	-	-	-	C	C	C
760360	C	C	C	-	-	-	-	C	761720	C	-	-	-	-	C	-	C
760400	C	C	-	C	C	C	C	C	761740	C	-	-	-	-	-	C	C
760420	C	C	-	C	C	C	-	C	761760	C	-	-	-	-	-	-	C
760440	C	C	-	C	C	-	C	C	762000	-	C	C	C	C	C	C	C
760460	C	C	-	C	C	-	-	C	762020	-	C	C	C	C	C	-	C
760500	C	C	-	C	-	C	C	C	762040	-	C	C	C	C	-	C	C
760520	C	C	-	C	-	C	-	C	762060	-	C	C	C	C	-	-	C
760540	C	C	-	C	-	-	C	C	762100	-	C	C	C	-	C	C	C
760560	C	C	-	C	-	-	-	C	762120	-	C	C	C	-	C	-	C
760600	C	C	-	-	C	C	C	C	762140	-	C	C	C	-	-	C	C
760620	C	C	-	-	C	C	-	C	762160	-	C	C	C	-	-	-	C
760640	C	C	-	-	C	-	C	C	762200	-	C	C	-	C	C	C	C
760660	C	C	-	-	C	-	-	C	762220	-	C	C	-	C	C	-	C
760700	C	C	-	-	-	C	C	C	762240	-	C	C	-	C	-	C	C
760720	C	C	-	-	-	C	-	C	762260	-	C	C	-	C	-	-	C
760740	C	C	-	-	-	-	C	C	762300	-	C	C	-	-	C	C	C
760760	C	C	-	-	-	-	-	C	762320	-	C	C	-	-	C	-	C
761000	C	-	C	C	C	C	C	C	762340	-	C	C	-	-	-	C	C
761020	C	-	C	C	C	C	-	C	762360	-	C	C	-	-	-	-	C
761040	C	-	C	C	C	-	C	C	762400	-	C	-	C	C	C	C	C
761060	C	-	C	C	C	-	-	C	762420	-	C	-	C	C	C	-	C
761100	C	-	C	C	-	C	C	C	762440	-	C	-	C	C	-	C	C
761120	C	-	C	C	-	C	-	C	762460	-	C	-	C	C	-	-	C
761140	C	-	C	C	-	-	C	C	762500	-	C	-	C	-	C	C	C
761160	C	-	C	C	-	-	-	C	762520	-	C	-	C	-	C	-	C
761200	C	-	C	-	C	C	C	C	762540	-	C	-	C	-	-	C	C
761220	C	-	C	-	C	C	-	C	762560	-	C	-	C	-	-	-	C
761240	C	-	C	-	C	-	C	C	762600	-	C	-	-	C	C	C	C
761260	C	-	C	-	C	-	-	C	762620	-	C	-	-	C	C	-	C
761300	C	-	C	-	-	C	C	C	762640	-	C	-	-	C	-	C	C
761320	C	-	C	-	-	C	-	C	762660	-	C	-	-	C	-	-	C
761340	C	-	C	-	-	-	C	C	762700	-	C	-	-	-	C	C	C

"-" = Open; "C" = Closed

10104X07 Table 3-4: DH Device Address Switch Settings

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DH STARTING ADDRESS	SWITCH 2 POSITIONS							
	8	7	6	5	4	3	2	1
762720	-	C	-	-	-	C	-	C
762740	-	C	-	-	-	-	C	C
762760	-	C	-	-	-	-	-	C
763000	-	-	C	C	C	C	C	C
763020	-	-	C	C	C	C	-	C
763040	-	-	C	C	C	-	C	C
763060	-	-	C	C	C	-	-	C
763100	-	-	C	C	-	C	C	C
763120	-	-	C	C	-	C	-	C
763140	-	-	C	C	-	-	C	C
763160	-	-	C	C	-	-	-	C
763200	-	-	C	-	C	C	C	C
763220	-	-	C	-	C	C	-	C
763240	-	-	C	-	C	-	C	C
763260	-	-	C	-	C	-	-	C
763300	-	-	C	-	-	C	C	C
763320	-	-	C	-	-	C	-	C
763340	-	-	C	-	-	-	C	C
763360	-	-	C	-	-	-	-	C
763400	-	-	-	C	C	C	C	C
763420	-	-	-	C	C	C	-	C
763440	-	-	-	C	C	-	C	C
763460	-	-	-	C	C	-	-	C
763500	-	-	-	C	-	C	C	C
763520	-	-	-	C	-	C	-	C
763540	-	-	-	C	-	-	C	C
763560	-	-	-	C	-	-	-	C
763600	-	-	-	-	C	C	C	C
763620	-	-	-	-	C	C	-	C
763640	-	-	-	-	C	-	C	C
763660	-	-	-	-	C	-	-	C
763700	-	-	-	-	-	C	C	C
763720	-	-	-	-	-	C	-	C
763740	-	-	-	-	-	-	C	C
763760	-	-	-	-	-	-	-	C

"-" = Open; "C" = Closed

Table 3-4: DH Device Address Switch Settings (con't.)

DM STARTING ADDRESS	SWITCH 1 POSITION							
	8	7	6	5	4	3	2	1
770400	C	C	C	C	C	C	C	C
770410	C	C	C	C	C	C	-	C
770420	C	C	C	C	C	-	C	C
770430	C	C	C	C	C	-	-	C
770440	C	C	C	C	-	C	C	C
770450	C	C	C	C	-	C	-	C
770460	C	C	C	C	-	-	C	C
770470	C	C	C	C	-	-	-	C
770500	C	C	C	-	C	C	C	C
770510	C	C	C	-	C	C	-	C
770520	C	C	C	-	C	-	C	C
770530	C	C	C	-	C	-	-	C
770540	C	C	C	-	-	C	C	C
770550	C	C	C	-	-	C	-	C
770560	C	C	C	-	-	-	C	C
770570	C	C	C	-	-	-	-	C
770600	C	C	-	C	C	C	C	C
770610	C	C	-	C	C	C	-	C
770620	C	C	-	C	C	-	C	C
770630	C	C	-	C	C	-	-	C
770640	C	C	-	C	-	C	C	C
770650	C	C	-	C	-	C	-	C
770660	C	C	-	C	-	-	C	C
770670	C	C	-	C	-	-	-	C
770700	C	C	-	-	C	C	C	C
770710	C	C	-	-	C	C	-	C
770720	C	C	-	-	C	-	C	C
770730	C	C	-	-	C	-	-	C
770740	C	C	-	-	-	C	C	C
770750	C	C	-	-	-	C	-	C
770760	C	C	-	-	-	-	C	C
770770	C	C	-	-	-	-	-	C

"-" = Open; "C" = Closed

Table 3-5: DM Device Address Switch Settings

DH VECTOR		SWITCH 5 POSITION						DH VECTOR		SWITCH 5 POSITION					
RECEIVE	TRANSMIT	8	7	6	5	4	3	RECEIVE	TRANSMIT	8	7	6	5	4	3
000	004	-	-	-	-	-	-	400	404	C	-	-	-	-	-
010	014	-	-	-	-	-	C	410	414	C	-	-	-	-	C
020	024	-	-	-	-	C	-	420	424	C	-	-	-	C	-
030	034	-	-	-	-	C	C	430	434	C	-	-	-	C	C
040	044	-	-	-	C	-	-	440	444	C	-	-	C	-	-
050	054	-	-	-	C	-	C	450	454	C	-	-	C	-	C
060	064	-	-	-	C	C	-	460	464	C	-	-	C	C	-
070	074	-	-	-	C	C	C	470	474	C	-	-	C	C	C
100	104	-	-	C	-	-	-	500	504	C	-	C	-	-	-
110	114	-	-	C	-	-	C	510	514	C	-	C	-	-	C
120	124	-	-	C	-	C	-	520	524	C	-	C	-	C	-
130	134	-	-	C	-	C	C	530	534	C	-	C	-	C	C
140	144	-	-	C	C	-	-	540	544	C	-	C	C	-	-
150	154	-	-	C	C	-	C	550	554	C	-	C	C	-	C
160	164	-	-	C	C	C	-	560	564	C	-	C	C	C	-
170	174	-	-	C	C	C	C	570	574	C	-	C	C	C	C
200	204	-	C	-	-	-	-	600	604	C	C	-	-	-	-
210	214	-	C	-	-	-	C	610	614	C	C	-	-	-	C
220	224	-	C	-	-	C	-	620	624	C	C	-	-	C	-
230	234	-	C	-	-	C	C	630	634	C	C	-	-	C	C
240	244	-	C	-	C	-	-	640	644	C	C	-	C	-	-
250	254	-	C	-	C	-	C	650	654	C	C	-	C	-	C
260	264	-	C	-	C	C	-	660	664	C	C	-	C	C	-
270	274	-	C	-	C	C	C	670	674	C	C	-	C	C	C
300	304	-	C	C	-	-	-	700	704	C	C	C	-	-	-
310	314	-	C	C	-	-	C	710	714	C	C	C	-	-	C
320	324	-	C	C	-	C	-	720	724	C	C	C	-	C	-
330	334	-	C	C	-	C	C	730	734	C	C	C	-	C	C
340	344	-	C	C	C	-	-	740	744	C	C	C	C	-	-
350	354	-	C	C	C	-	C	750	754	C	C	C	C	-	C
360	364	-	C	C	C	C	-	760	764	C	C	C	C	C	-
370	374	-	C	C	C	C	C	770	774	C	C	C	C	C	C

"-" = Open; "C" = Closed

Table 3-6: DH Vector Address Switch Settings

DM VECTOR	SWITCH 6 POSITION 8 7 6 5 4 3 2	DM VECTOR	SWITCH 6 POSITION 8 7 6 5 4 3 2	DM VECTOR	SWITCH 6 POSITION 8 7 6 5 4 3 2
000	- - - - - - -	254	- C - C - C C	530	C - C - C C -
004	- - - - - - C	260	- C - C C - -	534	C - C - C C C
010	- - - - - C -	264	- C - C C - C	540	C - C C - - -
014	- - - - - C C	270	- C - C C C -	544	C - C C - - C
020	- - - - C - -	274	- C - C C C C	550	C - C C - C -
024	- - - - C - C	300	- C C - - - -	554	C - C C - C C
030	- - - - C C -	304	- C C - - - C	560	C - C C C - -
034	- - - - C C C	310	- C C - - C -	564	C - C C C - C
040	- - - C - - -	314	- C C - - C C	570	C - C C C C -
044	- - - C - - C	320	- C C - C - -	574	C - C C C C C
050	- - - C - C -	324	- C C - C - C	600	C C - - - - -
054	- - - C - C C	330	- C C - C C -	604	C C - - - - C
060	- - - C C - -	334	- C C - C C C	610	C C - - - C -
064	- - - C C - C	340	- C C C - - -	614	C C - - - C C
070	- - - C C C -	344	- C C C - - C	620	C C - - C - -
074	- - - C C C C	350	- C C C - C -	624	C C - - C - C
100	- - C - - - -	354	- C C C - C C	630	C C - - C C -
104	- - C - - - C	360	- C C C C - -	634	C C - - C C C
110	- - C - - C -	364	- C C C C - C	640	C C - C - - -
114	- - C - - C C	370	- C C C C C -	644	C C - C - - C
120	- - C - C - -	374	- C C C C C C	650	C C - C - C -
124	- - C - C - C	400	C - - - - - -	654	C C - C - C C
130	- - C - C C -	404	C - - - - - C	660	C C - C C - -
134	- - C - C C C	410	C - - - - C -	664	C C - C C - C
140	- - C C - - -	414	C - - - - C C	670	C C - C C C -
144	- - C C - - C	420	C - - - C - -	674	C C - C C C C
150	- - C C - C -	424	C - - - C - C	700	C C C - - - -
154	- - C C - C C	430	C - - - C C -	704	C C C - - - C
160	- - C C C - -	434	C - - - C C C	710	C C C - - C -
164	- - C C C - C	440	C - - C - - -	714	C C C - - C C
170	- - C C C C -	444	C - - C - - C	720	C C C - C - -
174	- - C C C C C	450	C - - C - C -	724	C C C - C - C
200	- C - - - - -	454	C - - C - C C	730	C C C - C C -
204	- C - - - - C	460	C - - C C - -	734	C C C - C C C
210	- C - - - C -	464	C - - C C - C	740	C C C C - - -
214	- C - - - C C	470	C - - C C C -	744	C C C C - - C
220	- C - - C - -	474	C - - C C C C	750	C C C C - C -
224	- C - - C - C	500	C - C - - - -	754	C C C C - C C
230	- C - - C C -	504	C - C - - - C	760	C C C C C - -
234	- C - - C C C	510	C - C - - C -	764	C C C C C - C
240	- C - C - - -	514	C - C - - C C	770	C C C C C C -
244	- C - C - - C	520	C - C - C - -	774	C C C C C C C
250	- C - C - C -	524	C - C - C - C		

"-" = Open; "C" = Closed

Table 3-7: DM Vector Address Switch Settings

3.7 OPTION SWITCHES

3.7.1 EXTERNAL B BAUD RATE SELECTION (S3, S4-POSITION 1)

The external B baud rate for the DH/DM is set using switch S3 and switch S4, position 1. Table 3-9 lists switch settings or baud rate selection. If the rate you desire is not listed in the table, find the low and high rate it falls between. Use the switch setting for the lower of the two rates. For example, if the baud rate you require is 646, it falls between speeds 645.2 and 647.9 on the table. The switches would be set according to the lower speed, or 645.2.

3.7.2 MISCELLANEOUS FUNCTIONS

Switch S4 contains a variety of functions for the DH/DM. Table 3-8 lists these functions.

SWITCH S4 POSITION	OPEN/CLOSED	FUNCTIONAL DESCRIPTION
1	X	This switch is used in setting the baud rate. Refer to Section 3.7.1
2	Closed	A closed switch will assert Data Terminal Ready on all lines.
2	Open	An open switch allows Data Terminal Ready to be controlled by the DM.
3	X	Open enables 20 MS silo delay, closed disables silo delay.
4	Open	This switch is reserved for future use. It should remain open at all times.
5	Open	This switch is reserved for future use. It should remain open at all times.
6	Open	This switch should remain open. If closed and in the micro maintenance mode (switch 6, position 1 closed), the NPR portion of the bus test will be executed.
7	Open	This switch should remain open. If closed and in the micro maintenance mode (switch 6, position 1 closed), the BR portion of the bus test will be executed.
8	Open	This switch should remain open. It detects that the cables are plugged into the maintenance connectors.

Table 3-8: Switch S4 Functions

NOTE: Switch positions 6, 7, and 8 must be set open if operating in the micro maintenance mode. When closed, these switches are used only for factory test.

S4	S3								
1	8	7	6	5	4	3	2	1	Low rate
C	O	O	O	O	O	O	O	O	150.0
C	O	O	O	O	O	O	O	C	155.0
C	O	O	O	O	O	O	C	O	155.6
C	O	O	O	O	O	O	C	C	156.2
C	O	O	O	O	O	C	O	O	156.8
C	O	O	O	O	O	C	O	C	157.5
C	O	O	O	O	O	C	C	O	158.1
C	O	O	O	O	O	C	C	C	158.7
C	O	O	O	O	C	O	O	O	159.4
C	O	O	O	O	C	O	O	C	160.0
C	O	O	O	O	C	O	C	O	160.6
C	O	O	O	O	C	O	C	C	161.3
C	O	O	O	O	C	C	O	O	162.0
C	O	O	O	O	C	C	O	C	162.6
C	O	O	O	O	C	C	C	O	163.3
C	O	O	O	O	C	C	C	C	164.0
C	O	O	O	C	O	O	O	O	164.7
C	O	O	O	C	O	O	O	C	165.3
C	O	O	O	C	O	O	C	O	166.0
C	O	O	O	C	O	O	C	C	166.7
C	O	O	O	C	O	C	O	O	167.4
C	O	O	O	C	O	C	O	C	168.2
C	O	O	O	C	O	C	C	O	168.9
C	O	O	O	C	O	C	C	C	169.6
C	O	O	O	C	C	O	O	O	170.3
C	O	O	O	C	C	O	O	C	171.1
C	O	O	O	C	C	O	C	O	171.8
C	O	O	O	C	C	O	C	C	172.5
C	O	O	O	C	C	C	O	O	173.3
C	O	O	O	C	C	C	O	C	174.1
C	O	O	O	C	C	C	C	O	174.8
C	O	O	O	C	C	C	C	C	175.6
C	O	O	C	O	O	O	O	O	176.4
C	O	O	C	O	O	O	O	C	177.2
C	O	O	C	O	O	O	C	O	178.0
C	O	O	C	O	O	O	C	C	178.8
C	O	O	C	O	O	C	O	O	179.6
C	O	O	C	O	O	C	O	C	180.4
C	O	O	C	O	O	C	C	O	181.2
C	O	O	C	O	O	C	C	C	182.1
C	O	O	C	O	C	O	O	O	182.9
C	O	O	C	O	C	O	O	C	183.8
C	O	O	C	O	C	O	C	O	184.6
C	O	O	C	O	C	O	C	C	185.5
C	O	O	C	O	C	C	O	O	186.4
C	O	O	C	O	C	C	O	C	187.2
C	O	O	C	O	C	C	C	O	188.1
C	O	O	C	O	C	C	C	C	189.0
C	O	O	C	C	O	O	O	O	189.9
C	O	O	C	C	O	O	O	C	190.8
C	O	O	C	C	O	O	C	O	191.8
C	O	O	C	C	O	O	C	C	192.7
C	O	O	C	C	O	C	O	O	193.6
C	O	O	C	C	O	C	O	C	194.6
C	O	O	C	C	O	C	C	O	195.6

S4	S3								
1	8	7	6	5	4	3	2	1	Low rate
C	O	O	C	C	O	C	C	C	196.5
C	O	O	C	C	C	O	O	O	197.5
C	O	O	C	C	C	O	O	C	198.5
C	O	O	C	C	C	O	C	O	199.5
C	O	O	C	C	C	O	C	C	200.5
C	O	O	C	C	C	C	O	O	201.5
C	O	O	C	C	C	C	O	C	202.6
C	O	O	C	C	C	C	C	O	203.6
C	O	O	C	C	C	C	C	C	204.7
C	O	C	O	O	O	O	O	O	205.7
C	O	C	O	O	O	O	O	C	206.8
C	O	C	O	O	O	O	C	O	207.9
C	O	C	O	O	O	O	C	C	209.0
C	O	C	O	O	O	C	O	O	210.1
C	O	C	O	O	O	C	O	C	211.2
C	O	C	O	O	O	C	C	O	212.3
C	O	C	O	O	O	C	C	C	213.5
C	O	C	O	O	C	O	O	O	214.6
C	O	C	O	O	C	O	O	C	215.8
C	O	C	O	O	C	O	C	O	217.0
C	O	C	O	O	C	O	C	C	218.2
C	O	C	O	O	C	C	O	O	219.4
C	O	C	O	O	C	C	O	C	220.6
C	O	C	O	O	C	C	C	O	221.9
C	O	C	O	O	C	C	C	C	223.1
C	O	C	O	C	O	O	O	O	224.4
C	O	C	O	C	O	O	O	C	225.6
C	O	C	O	C	O	O	C	O	226.9
C	O	C	O	C	O	O	C	C	228.2
C	O	C	O	C	O	C	O	O	229.6
C	O	C	O	C	O	C	O	C	230.9
C	O	C	O	C	O	C	C	O	232.3
C	O	C	O	C	O	C	C	C	233.6
C	O	C	O	C	C	O	O	O	235.0
C	O	C	O	C	C	O	O	C	236.4
C	O	C	O	C	C	O	C	O	237.8
C	O	C	O	C	C	O	C	C	239.3
C	O	C	O	C	C	C	O	O	240.7
C	O	C	O	C	C	C	O	C	242.2
C	O	C	O	C	C	C	C	O	243.7
C	O	C	O	C	C	C	C	C	245.2
C	O	C	C	O	O	O	O	O	246.7
C	O	C	C	O	O	O	O	C	248.3
C	O	C	C	O	O	O	C	O	249.8
C	O	C	C	O	O	O	C	C	251.4
C	O	C	C	O	O	C	O	O	253.0
C	O	C	C	O	O	C	O	C	254.7
C	O	C	C	O	O	C	C	O	256.3
C	O	C	C	O	O	C	C	C	258.0
C	O	C	C	O	C	O	O	O	259.7
C	O	C	C	O	C	O	O	C	261.4
C	O	C	C	O	C	O	C	O	263.1
C	O	C	C	O	C	O	C	C	264.9
C	O	C	C	O	C	C	O	O	266.7
C	O	C	C	O	C	C	O	C	268.5

Table 3-9: Baud Rate Switch Settings

S4	S3								
1	8	7	6	5	4	3	2	1	Low rate
C	O	C	C	O	C	C	C	O	270.3
C	O	C	C	O	C	C	C	C	272.2
C	O	C	C	C	O	O	O	O	274.1
C	O	C	C	C	O	O	O	C	276.0
C	O	C	C	C	O	O	C	O	277.9
C	O	C	C	C	O	O	C	C	279.9
C	O	C	C	C	O	C	O	O	281.9
C	O	C	C	C	O	C	O	C	283.9
C	O	C	C	C	O	C	C	O	285.9
C	O	C	C	C	O	C	C	C	288.0
C	O	C	C	C	C	O	O	O	290.1
C	O	C	C	C	C	O	O	C	292.3
C	O	C	C	C	C	O	C	O	294.4
C	O	C	C	C	C	O	C	C	296.6
C	O	C	C	C	C	C	O	O	298.9
C	O	C	C	C	C	C	O	C	301.1
C	O	C	C	C	C	C	C	O	303.5
C	O	C	C	C	C	C	C	C	305.8
C	C	O	O	O	O	O	O	O	308.2
C	C	O	O	O	O	O	O	C	310.6
C	C	O	O	O	O	O	C	O	313.0
C	C	O	O	O	O	O	C	C	315.5
C	C	O	O	O	O	C	O	O	318.1
C	C	O	O	O	O	C	O	C	320.7
C	C	O	O	O	O	C	C	O	323.3
C	C	O	O	O	O	C	C	C	325.9
C	C	O	O	O	C	O	O	O	328.6
C	C	O	O	O	C	O	O	C	331.4
C	C	O	O	O	C	O	C	O	334.2
C	C	O	O	O	C	O	C	C	337.0
C	C	O	O	O	C	C	O	O	339.9
C	C	O	O	O	C	C	O	C	342.9
C	C	O	O	O	C	C	C	O	345.9
C	C	O	O	O	C	C	C	C	348.9
C	C	O	O	C	O	O	O	O	352.0
C	C	O	O	C	O	O	O	C	355.2
C	C	O	O	C	O	O	C	O	358.4
C	C	O	O	C	O	O	C	C	361.7
C	C	O	O	C	O	C	O	O	365.0
C	C	O	O	C	O	C	O	C	368.4
C	C	O	O	C	O	C	C	O	371.8
C	C	O	O	C	O	C	C	C	375.4
C	C	O	O	C	C	O	O	O	379.0
C	C	O	O	C	C	O	O	C	382.6
C	C	O	O	C	C	O	C	O	386.4
C	C	O	O	C	C	O	C	C	390.2
C	C	O	O	C	C	C	O	O	394.0
C	C	O	O	C	C	C	O	C	398.0
C	C	O	O	C	C	C	C	O	402.0
C	C	O	O	C	C	C	C	C	406.2
C	C	O	C	O	O	O	O	O	410.4
C	C	O	C	O	O	O	O	C	414.7
C	C	O	C	O	O	O	C	O	419.1
C	C	O	C	O	O	O	C	C	423.5
C	C	O	C	O	O	C	O	O	428.1

S4	S3								
1	8	7	6	5	4	3	2	1	Low rate
C	C	O	C	O	O	C	O	C	432.8
C	C	O	C	O	O	C	C	O	437.6
C	C	O	C	O	O	C	C	C	442.5
C	C	O	C	O	C	O	O	O	447.5
C	C	O	C	O	C	O	O	C	452.6
C	C	O	C	O	C	O	C	O	457.8
C	C	O	C	O	C	O	C	C	463.2
C	C	O	C	O	C	C	O	O	468.7
C	C	O	C	O	C	C	O	C	474.3
C	C	O	C	O	C	C	C	O	480.0
C	C	O	C	O	C	C	C	C	485.9
C	C	O	C	C	O	O	O	O	491.9
C	C	O	C	C	O	O	O	C	498.1
C	C	O	C	C	O	O	C	O	504.5
C	C	O	C	C	O	O	C	C	511.0
C	C	O	C	C	O	C	O	O	517.7
C	C	O	C	C	O	C	O	C	524.5
C	C	O	C	C	O	C	C	O	531.6
C	C	O	C	C	O	C	C	C	538.8
C	C	O	C	C	C	O	O	O	546.2
C	C	O	C	C	C	O	O	C	553.9
C	C	O	C	C	C	O	C	O	561.7
C	C	O	C	C	C	O	C	C	569.8
C	C	O	C	C	C	C	O	O	578.1
C	C	O	C	C	C	C	O	C	586.7
C	C	O	C	C	C	C	C	O	595.5
C	C	O	C	C	C	C	C	C	604.6
O	O	O	O	O	O	O	O	O	614.0
O	O	O	O	O	O	O	O	C	620.0
O	O	O	O	O	O	O	C	O	622.4
O	O	O	O	O	O	O	C	C	624.9
O	O	O	O	O	O	C	O	O	627.3
O	O	O	O	O	O	C	O	C	629.8
O	O	O	O	O	O	C	C	O	632.3
O	O	O	O	O	O	C	C	C	634.9
O	O	O	O	O	C	O	O	O	637.4
O	O	O	O	O	C	O	O	C	640.0
O	O	O	O	O	C	O	C	O	642.6
O	O	O	O	O	C	O	C	C	645.2
O	O	O	O	O	C	C	O	O	647.9
O	O	O	O	O	C	C	O	C	650.5
O	O	O	O	O	C	C	C	O	653.2
O	O	O	O	O	C	C	C	C	655.9
O	O	O	O	C	O	O	O	O	658.6
O	O	O	O	C	O	O	O	C	661.4
O	O	O	O	C	O	O	C	O	664.2
O	O	O	O	C	O	O	C	C	667.0
O	O	O	O	C	O	C	O	O	669.8
O	O	O	O	C	O	C	O	C	672.6
O	O	O	O	C	O	C	C	O	675.5
O	O	O	O	C	O	C	C	C	678.4
O	O	O	O	C	C	O	O	O	681.3
O	O	O	O	C	C	O	O	C	684.2
O	O	O	O	C	C	O	C	O	687.2
O	O	O	O	C	C	O	C	C	690.2

Table 3-9: Baud Rate Switch Settings (Con't.)

S4	S3								
1	8	7	6	5	4	3	2	1	Low rate
O	O	O	O	C	C	C	O	O	693.2
O	O	O	O	C	C	C	O	C	696.3
O	O	O	O	C	C	C	C	O	699.3
O	O	O	O	C	C	C	C	C	702.4
O	O	O	C	O	O	O	O	O	705.6
O	O	O	C	O	O	O	O	C	708.7
O	O	O	C	O	O	O	C	O	711.9
O	O	O	C	O	O	O	C	C	715.1
O	O	O	C	O	O	C	O	O	718.4
O	O	O	C	O	O	C	O	C	721.6
O	O	O	C	O	O	C	C	O	724.9
O	O	O	C	O	O	C	C	C	728.3
O	O	O	C	O	C	O	O	O	731.6
O	O	O	C	O	C	O	O	C	735.0
O	O	O	C	O	C	O	C	O	738.5
O	O	O	C	O	C	O	C	C	741.9
O	O	O	C	O	C	C	O	O	745.4
O	O	O	C	O	C	C	O	C	748.9
O	O	O	C	O	C	C	C	O	752.5
O	O	O	C	O	C	C	C	C	756.1
O	O	O	C	C	O	O	O	O	759.7
O	O	O	C	C	O	O	O	C	763.4
O	O	O	C	C	O	O	C	O	767.1
O	O	O	C	C	O	O	C	C	770.8
O	O	O	C	C	O	C	O	O	774.6
O	O	O	C	C	O	C	O	C	778.4
O	O	O	C	C	O	C	C	O	782.2
O	O	O	C	C	O	C	C	C	786.1
O	O	O	C	C	C	O	O	O	790.0
O	O	O	C	C	C	O	O	C	794.0
O	O	O	C	C	C	O	C	O	798.0
O	O	O	C	C	C	O	C	C	802.0
O	O	O	C	C	C	C	O	O	806.1
O	O	O	C	C	C	C	O	C	810.2
O	O	O	C	C	C	C	C	O	814.4
O	O	O	C	C	C	C	C	C	818.6
O	O	C	O	O	O	O	O	O	822.9
O	O	C	O	O	O	O	O	C	827.2
O	O	C	O	O	O	O	C	O	831.5
O	O	C	O	O	O	O	C	C	835.9
O	O	C	O	O	O	C	O	O	840.3
O	O	C	O	O	O	C	O	C	844.8
O	O	C	O	O	O	C	C	O	849.3
O	O	C	O	O	O	C	C	C	853.9
O	O	C	O	O	C	O	O	O	858.5
O	O	C	O	O	C	O	O	C	863.2
O	O	C	O	O	C	O	C	O	868.0
O	O	C	O	O	C	O	C	C	872.7
O	O	C	O	O	C	C	O	O	877.6
O	O	C	O	O	C	C	O	C	882.5
O	O	C	O	O	C	C	C	O	887.4
O	O	C	O	O	C	C	C	C	892.4
O	O	C	O	C	O	O	O	O	897.5
O	O	C	O	C	O	O	O	C	902.6
O	O	C	O	C	O	O	C	O	907.7

S4	S3								
1	8	7	6	5	4	3	2	1	Low rate
O	O	C	O	C	O	O	C	C	913.0
O	O	C	O	C	O	C	O	O	918.3
O	O	C	O	C	O	C	O	C	923.6
O	O	C	O	C	O	C	C	O	929.0
O	O	C	O	C	O	C	C	C	934.5
O	O	C	O	C	C	O	O	O	940.1
O	O	C	O	C	C	O	O	C	945.7
O	O	C	O	C	C	O	C	O	951.4
O	O	C	O	C	C	O	C	C	957.1
O	O	C	O	C	C	C	O	O	962.9
O	O	C	O	C	C	C	O	C	968.8
O	O	C	O	C	C	C	C	O	974.8
O	O	C	O	C	C	C	C	C	980.8
O	O	C	C	O	O	O	O	O	986.9
O	O	C	C	O	O	O	O	C	993.1
O	O	C	C	O	O	O	C	O	999.4
O	O	C	C	O	O	O	C	C	1,006
O	O	C	C	O	O	C	O	O	1,012
O	O	C	C	O	O	C	O	C	1,019
O	O	C	C	O	O	C	C	O	1,025
O	O	C	C	O	O	C	C	C	1,032
O	O	C	C	O	C	O	O	O	1,039
O	O	C	C	O	C	O	O	C	1,046
O	O	C	C	O	C	O	C	O	1,053
O	O	C	C	O	C	O	C	C	1,060
O	O	C	C	O	C	C	O	O	1,067
O	O	C	C	O	C	C	O	C	1,074
O	O	C	C	O	C	C	C	O	1,081
O	O	C	C	O	C	C	C	C	1,089
O	O	C	C	C	O	O	O	O	1,096
O	O	C	C	C	O	O	O	C	1,104
O	O	C	C	C	O	O	C	O	1,112
O	O	C	C	C	O	O	C	C	1,119
O	O	C	C	C	O	C	O	O	1,127
O	O	C	C	C	O	C	O	C	1,135
O	O	C	C	C	O	C	C	O	1,144
O	O	C	C	C	O	C	C	C	1,152
O	O	C	C	C	C	O	O	O	1,160
O	O	C	C	C	C	O	O	C	1,169
O	O	C	C	C	C	O	C	O	1,178
O	O	C	C	C	C	O	C	C	1,187
O	O	C	C	C	C	C	O	O	1,195
O	O	C	C	C	C	C	O	C	1,205
O	O	C	C	C	C	C	C	O	1,214
O	O	C	C	C	C	C	C	C	1,223
O	C	O	O	O	O	O	O	O	1,233
O	C	O	O	O	O	O	O	C	1,242
O	C	O	O	O	O	O	C	O	1,252
O	C	O	O	O	O	O	C	C	1,262
O	C	O	O	O	O	C	O	O	1,272
O	C	O	O	O	O	C	O	C	1,283
O	C	O	O	O	O	C	C	O	1,293
O	C	O	O	O	O	C	C	C	1,304
O	C	O	O	O	C	O	O	O	1,315
O	C	O	O	O	C	O	O	C	1,326

Table 3-9: Baud Rate Switch Settings (Con't.)

S4	S3								
1	8	7	6	5	4	3	2	1	Low rate
O	C	O	O	O	C	O	C	O	1,337
O	C	O	O	O	C	O	C	C	1,348
O	C	O	O	O	C	C	O	O	1,360
O	C	O	O	O	C	C	O	C	1,371
O	C	O	O	O	C	C	C	O	1,383
O	C	O	O	O	C	C	C	C	1,396
O	C	O	O	C	O	O	O	O	1,408
O	C	O	O	C	O	O	O	C	1,421
O	C	O	O	C	O	O	C	O	1,434
O	C	O	O	C	O	O	C	C	1,447
O	C	O	O	C	O	C	O	O	1,460
O	C	O	O	C	O	C	O	C	1,474
O	C	O	O	C	O	C	C	O	1,487
O	C	O	O	C	O	C	C	C	1,501
O	C	O	O	C	C	O	O	O	1,516
O	C	O	O	C	C	O	O	C	1,530
O	C	O	O	C	C	O	C	O	1,545
O	C	O	O	C	C	O	C	C	1,561
O	C	O	O	C	C	C	O	O	1,576
O	C	O	O	C	C	C	O	C	1,592
O	C	O	O	C	C	C	C	O	1,608
O	C	O	O	C	C	C	C	C	1,625
O	C	O	C	O	O	O	O	O	1,641
O	C	O	C	O	O	O	O	C	1,659
O	C	O	C	O	O	O	C	O	1,676
O	C	O	C	O	O	O	C	C	1,694
O	C	O	C	O	O	C	O	O	1,712
O	C	O	C	O	O	C	O	C	1,731
O	C	O	C	O	O	C	C	O	1,750
O	C	O	C	O	O	C	C	C	1,770
O	C	O	C	O	C	O	O	O	1,790
O	C	O	C	O	C	O	O	C	1,810
O	C	O	C	O	C	O	C	O	1,831
O	C	O	C	O	C	O	C	C	1,853
O	C	O	C	O	C	C	O	O	1,875
O	C	O	C	O	C	C	O	C	1,897
O	C	O	C	O	C	C	C	O	1,920
O	C	O	C	O	C	C	C	C	1,944
O	C	O	C	C	O	O	O	O	1,968
O	C	O	C	C	O	O	O	C	1,993
O	C	O	C	C	O	O	C	O	2,018
O	C	O	C	C	O	O	C	C	2,044
O	C	O	C	C	O	C	O	O	2,071
O	C	O	C	C	O	C	O	C	2,098
O	C	O	C	C	O	C	C	O	2,126
O	C	O	C	C	O	C	C	C	2,155
O	C	O	C	C	C	O	O	O	2,185
O	C	O	C	C	C	O	O	C	2,215
O	C	O	C	C	C	O	C	O	2,247
O	C	O	C	C	C	O	C	C	2,279
O	C	O	C	C	C	C	O	O	2,313
O	C	O	C	C	C	C	O	C	2,347
O	C	O	C	C	C	C	C	O	2,382
O	C	O	C	C	C	C	C	C	2,418
O	C	C	O	O	O	O	O	O	2,456

S4	S3								
1	8	7	6	5	4	3	2	1	Low rate
O	C	C	O	O	O	O	O	C	2,495
O	C	C	O	O	O	O	C	O	2,535
O	C	C	O	O	O	O	C	C	2,576
O	C	C	O	O	O	C	O	O	2,618
O	C	C	O	O	O	C	O	C	2,662
O	C	C	O	O	O	C	C	O	2,708
O	C	C	O	O	O	C	C	C	2,755
O	C	C	O	O	C	O	O	O	2,804
O	C	C	O	O	C	O	O	C	2,854
O	C	C	O	O	C	O	C	O	2,907
O	C	C	O	O	C	O	C	C	2,961
O	C	C	O	O	C	C	O	O	3,017
O	C	C	O	O	C	C	O	C	3,076
O	C	C	O	O	C	C	C	O	3,137
O	C	C	O	O	C	C	C	C	3,200
O	C	C	O	C	O	O	O	O	3,266
O	C	C	O	C	O	O	O	C	3,335
O	C	C	O	C	O	O	C	O	3,407
O	C	C	O	C	O	O	C	C	3,482
O	C	C	O	C	O	C	O	O	3,560
O	C	C	O	C	O	C	O	C	3,642
O	C	C	O	C	O	C	C	O	3,728
O	C	C	O	C	O	C	C	C	3,817
O	C	C	O	C	C	O	O	O	3,912
O	C	C	O	C	C	O	O	C	4,011
O	C	C	O	C	C	O	C	O	4,115
O	C	C	O	C	C	O	C	C	4,225
O	C	C	O	C	C	C	O	O	4,341
O	C	C	O	C	C	C	O	C	4,463
O	C	C	O	C	C	C	C	O	4,592
O	C	C	O	C	C	C	C	C	4,729
O	C	C	C	O	O	O	O	O	4,875
O	C	C	C	O	O	O	O	C	5,030
O	C	C	C	O	O	O	C	O	5,195
O	C	C	C	O	O	O	C	C	5,371
O	C	C	C	O	O	C	O	O	5,560
O	C	C	C	O	O	C	O	C	5,762
O	C	C	C	O	O	C	C	O	5,979
O	C	C	C	O	O	C	C	C	6,214
O	C	C	C	O	C	O	O	O	6,468
O	C	C	C	O	C	O	O	C	6,743
O	C	C	C	O	C	O	C	O	7,043
O	C	C	C	O	C	O	C	C	7,371
O	C	C	C	O	C	C	O	O	7,731
O	C	C	C	O	C	C	O	C	8,128
O	C	C	C	O	C	C	C	O	8,568
O	C	C	C	O	C	C	C	C	9,059
O	C	C	C	C	O	O	O	O	9,609
O	C	C	C	C	O	O	O	C	10,230

Table 3-9 : Baud Rate Switch Settings (Con't.)

3.8 MAINTENANCE FEATURES

3.8.1 MAINTENANCE FEATURES

For maintenance purposes, the DH/DM contains three switch positions to control the resident microcoded diagnostic. The switch positions are switch S5, positions 1 and 2, and switch S6, position 1. Refer to Table 3-10 for definitions and functions of these switches. Table 3-11 lists the execution sequence of the microdiagnostic.

For normal operation, set the switches as follows:

Switch S5, position 1 - CLOSED
Switch S5, position 2 - OPEN
Switch S6, position 1 - OPEN

	SWITCH S6	SWITCH S5		
	1	2	1	FUNCTIONAL DESCRIPTION
Open	OPEN	X	OPEN	Run microdiagnostic, omit Bus and UART section, exit to emulation after end of test or first error.
Normal	OPEN	X	CLOSED	Run microdiagnostic, omit Bus and UART section, exit to emulation if no errors. Will not proceed to emulation routine if an error is detected.
Micro Maintenance	CLOSED	OPEN	OPEN	Loop in entire microdiagnostic test, including the Bus and UART section. Will not enter emulation.
	CLOSED	OPEN	CLOSED	Hang in section if error occurs. Will not enter emulation. LED 1, 2, and 3 will display section error has occured in. ERR LED will display error, if any.
	CLOSED	CLOSED	OPEN	Loop on section. Will not proceed into another section or into emulation. LED 1, 2, and 3 will display section. ERR LED will display error, if any.
	CLOSED	CLOSED	CLOSED	Loop on section, hang if error. Will not proceed into emulation. LED 1, 2, and 3 will display section. ERR LED will display error, if any.

Table 3-10: Maintenance Switch Settings
(See notes on following page.)

NOTE: 1. Bus and UART section are bypassed when switches are set to proceed into emulation due to the time required to perform the UART test, and because the Bus tests may disturb the system.

2. Any error detected in the first section of the microdiagnostic will cause a hang regardless of the switch settings.

3. The "ERR" indicator is reset at the beginning of each section of the microdiagnostic.

EXECUTION SEQUENCE	SECTION (As encoded in LEDs)
Power Up	
1	Section 7 - SEQ
2	Section 3 - DATA (2901)
3	Section 1 - DBIT
4	Section 5 - PROM
5	Section 4 - BUF
6	Section 6 - BUS (NPR, BR)
7	Section 2 - UART If S5-1 is open, Section 6 and 2 are bypassed and emulation is entered after Section 4.

Table 3-11: Microdiagnostic Execution Chart

3.8.2 MAINTENANCE DISPLAY

The DH/DM contains four LEDs for maintenance display purposes. These LEDs are located at the top of the board, between connectors J1 and J2. Figure 3-1 shows the location of the LEDs. Refer to Table 3-12 for descriptions of the LED displays. Section 3.13 provides more information on the LEDs.

DISPLAY				DESCRIPTION
ERR	1	2	3	
off	off	off	off	END PASS / EMULATION
off	off	off	on	Testing Section 1 - DBIT
off	off	on	off	Testing Section 2 - UART
off	off	on	on	Testing Section 3 - DATA (2901)
off	on	off	off	Testing Section 4 - BUF
off	on	off	on	Testing Section 5 - PROM
off	on	on	off	Testing Section 6 - BUS (NPR, BR)
off	on	on	on	Testing Section 7 - SEQ
on	off	off	off	Error - Undefined problem
on	off	off	on	Error in Section 1 - DBIT Error
on	off	on	off	Error in Section 2 - UART Error
on	off	on	on	Error in Section 3 - DATA (2901) Error
on	on	off	off	Error in Section 4 - Error BUF
on	on	off	on	Error in Section 5 - Error PROM
on	on	on	off	Error in Section 6 - Error BUS
on	on	on	on	Error in Section 7 - SEQ Error

Table 3-12: Maintenance Display Chart

3.9 PRIORITY SELECTION

The standard priority interrupt levels for the DH/DM are BG5 for the DH and BG4 for the DM. These levels are factory wired and require no user adjustment.

If you wish to change interrupt levels for the DH or DM, use the strapping chart in Appendix A.

3.10 PREPARING YOUR SYSTEM FOR THE DH/DM

To prepare your system for installing the DH/DM, remove power from the system. Use either the front panel switch or the master breaker switch at the bottom of the cabinet. We suggest that both switches be turned off.

Once power is removed from the system, locate a vacant hex SPC slot that can accomodate the DH/DM board. Normally, this will be slots two or three in the DD11-C four slot backplane, or slots two through eight of the DD11-D nine slot backplane. Remove any previously installed bus grant continuity cards from this slot. If using a DEC backplane, modify the backplane to accomodate DH/DM by removing the wire between pins CA1 and CB1 of that slot.

3.11 HOW TO INSTALL THE DH/DM INTO YOUR SYSTEM

3.11.1 BOARD INSTALLATION

Prior to installing the DH/DM board, verify that the address and vector switches are set to the desired settings. Insert the board into the selected vacant slot, using the card guides to ensure that it is properly positioned. Insert the board until the two card extractor devices on the DH/DM can be used to further insert the board into the SPC connector blocks.

3.11.2 EIA PANEL INSTALLATION

The EIA panel is usually mounted at the rear of the computer cabinet to allow easy access to panel controls. Four mounting locations are provided to mount the panel directly into the cabinet. If preferred, right angle brackets are supplied to recess the panel.

3.11.3 INTERCONNECTING CABLE INSTALLATION

Locate the cable end marked "Panel" and connect it to the distribution panel connector J3 by aligning the triangles during insertion.

CAUTION

Align the triangles on the cable connectors with the triangles on the connectors on the board or panel. EXTENSIVE DAMAGE MAY RESULT FROM ANY MISALIGNMENT.

Attach the other end of this cable to connector J1 on the DH/DM board by aligning the triangles during insertion. Locate the end marked "Panel" on the second cable and connect it to the distribution panel connector J4 by aligning the triangles during insertion. Attach the other end of this cable to connector J2 on the DH/DM board by aligning the triangles during insertion.

3.12 DIAGNOSTICS

The following diagnostics can be used to verify operation of DH/DM and/or your system.

ZDHM — This test program is designed to aid in acceptance testing, installation checkout, and corrective maintenance. It consists of 48 logically sequenced diagnostic tests which verify that the DH/DM is operating in accordance with its design specifications.

DEC/X11 — This program provides the means to generate, run, control, and update interactive hardware system exerciser programs for PDP-11 systems.

Single Line Echo Test	Tests any line by using an asynchronous terminal device. Operates in send mode and echo mode.
Data Patterns/Cable Test	Tests any line using an H315 test connector to terminate the line under test. This program would normally be used for troubleshooting a specific problem.

Running these first three diagnostics will verify completely the operation of DH/DM. The following diagnostics are all contained in ZDHM and can be used when it is not available.

ZDHA This program tests the correct function of all read/write bits in the system control register, line parameter register, break control register, and silo status register. Additionally, it checks the function of read-only bits in maintenance mode, register addressability, and the function of master clear. Each function is tested in an individual test loop.

ZDHB This program tests the byte count and bus address memories of the DH/DM. Each memory is tested for addressability and data read/write capability.

ZDHC This program checks the basic transmitter and receiver functions. These functions include interrupts, transmitter NPR logic, and receiver silo logic.

ZDHD This program verifies proper operation of speed selection functions of the line parameter for each transmitter and receiver line. Transmitter timing is checked first, and then receiver timing. The program uses a relative timing comparison to determine if line speed selection is correct.

ZDHE This program verifies that character length on each line can be selected correctly, and the correct line number and character status are received on each line selected for transmission.

ZDHF This test verifies that each line can transmit and receive all 256 combinations of characters (8 bits per character) at all speeds. It also verifies that each line can transmit and receive all character lengths (8-5) at a speed of 9600 baud.

ZDHG This test checks that the parity error flag asserts for all 16 lines of the DH/DM, one line at a time. The test transmits binary count patterns of all 16 lines simultaneously. The test also verifies parity generation logic and parity reception logic (odd and even parity for 5, 6, 7, and 8 level codes).

3.13 INSTALLATION VERIFICATION

Once the DH/DM has been installed into the system, power can be applied. During the power-up sequence, the DH/DM performs an internal diagnostic. This diagnostic verifies the majority of internal operations of the DH/DM. With the maintenance switch set for normal operation, it does not check circuitry that is used to interface to the Unibus.

The diagnostic mode is switch selectable. Refer to Section 3.8 for proper switch settings.

By monitoring four LEDs near the top of the board, proper internal operation of the DH/DM can be verified. Figure 3-1 shows the location of the LEDs. When power is applied, all four LEDs should light up and after a very short flash, should all turn off. Any LED which remains lit indicates a malfunction and requires investigation. Table 3-12 supplies the definitions of the four LEDs and Section 4 provides troubleshooting tips in case an LED remains lit.

If all four LED displays turn off after power has been applied to the system, address the DH/DM through the operator front panel or ODT. Examine the second address assigned to the DH/DM, (address 76XXX2 is the NRCR register) which contains the DH and DM vector selection information. Refer to Figure 3-4 for switch verification. If the vector settings are incorrect or the device does not respond, verify the vector and address settings as described in Section 3.5 Repeat the above operation.

If the micro-diagnostic passes, and the address and vector settings have been verified, continue to verify installation of the DH/DM by executing the software diagnostic. The ZDHM diagnostic can be loaded and executed at location 200. It automatically auto-sizes to determine the number of DH/DM's in the system and performs verification of the DH/DM in the external loop-back mode. The diagnostic also prints the address and vector assignments, if front panel switch register 1 is on. Compare these with your selections to verify correct address and vector assignments.

NOTE: Prior to running the diagnostics, except DECX/11, the cables must be installed in maintenance connectors J7 and J8 on the distribution panel. Figure 3-5 shows cables installed in maintenance connectors.

Further information on operation of the diagnostic can be found in the diagnostic listing. Proper performance of the diagnostic will be indicated by pass counts displayed on the operator terminal. We suggest running at least two passes. Once the diagnostic has been verified, return the cables to their normal connectors.

If your system adequately performs these diagnostics, DH/DM installation is verified and ready for use with your operating system.

If any errors occur in the ZDHM diagnostic, analyze the error printout. If the error is in the DH/DM address space, verify the switch settings. If the system still fails, contact our Product Support group as described in Section 4.

If DECX/11 fails, try to use operator selections to isolate the problem. If DH/DM seems to be the source of the error, verify the steps in Section 3 again. If the problem persists, contact the Able Product Support group as described in Section 4. So we can be more responsive to your needs, keep the error printout on hand when calling us.

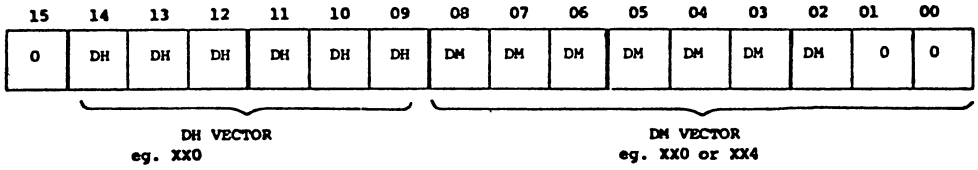

Figure 3-4: Next Received Character Register (NRCR)

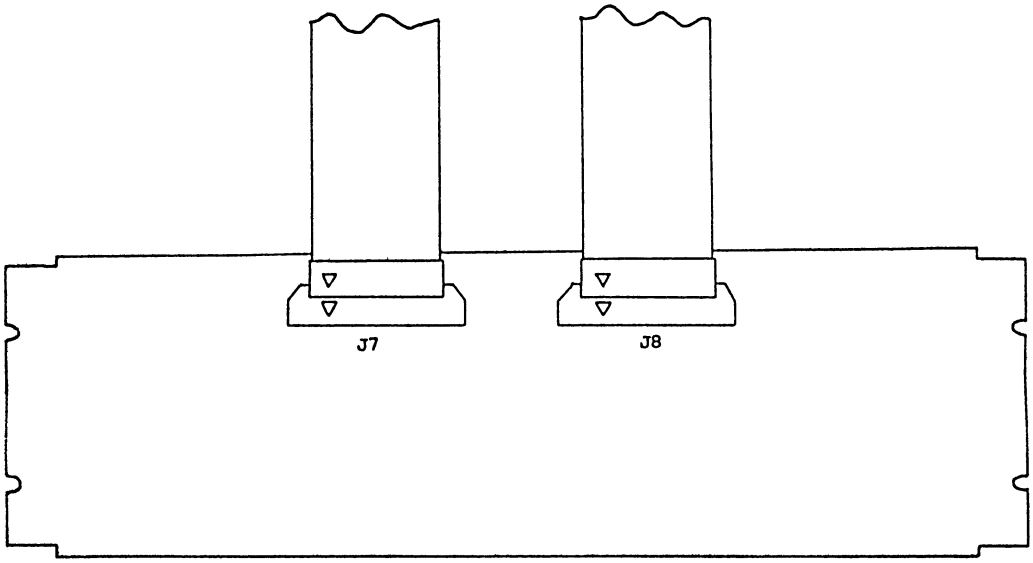

Figure 3-5: Cables Installed For Maintenance Mode

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SECTION 4
WHAT TO DO IF DH/DM DOES NOT WORK

4.1 HOW TO CARE FOR DH/DM

ABLE products are designed to provide years of service with a minimum of care. Here are a few tips to help you avoid problems.

- If a printed circuit board is frequently inserted and removed, it tends to build up a gum-like residue on the contacts. Clean this residue off using alcohol or freon. Use of a pencil eraser can remove some of the gold on the contacts, so if you choose to use one, go easy.

- Every six months remove each printed circuit board and clean off any accumulated dust. Dust can impede air flow. While the board is out, inspect it for any visual evidence of a potential problem such as damaged components, loose connections, etc.

- Schematics for your DH/DM can be ordered from the ABLE factory. Document numbers are listed below.

10103003	DH/DM PC Board
10114003	EIA Distribution Panel

- If you wish to maintain a spare parts inventory, refer to the recommended list in Appendix C.

- If a problem arises with the operation of your DH/DM, follow the steps outlined in the following sections.

4.2 TROUBLESHOOTING TIPS

4.2.1 "ERR" LED ON

When the ERR LED remains lit, a failure in the micro-diagnostics is indicated. We suggest that you run the power-up sequence a few times to verify consistency of the ERR failure. Be sure to verify the switch settings contained in Table 3-8 and Table 3-10.

If ERR continues to remain lit, your DH/DM unit can be considered faulty. If so, contact the ABLE Product Support Center as outlined in Section 4.3 and 4.4.

An optional switch setting has been provided which allows progression into the emulation mode if an ERR has occured in the micro-diagnostic. Table 3-10 provides information on how to set this switch.

In any case, an ERR failure should be reported to the ABLE Product Support Center so that it can be evaluated and resolved.

4.2.2 VERIFY CONFIGURATION AND INSTALLATION

Experience has shown that the greatest number of problems with DH/DM involve configuration or installation errors. An address, vector, or priority level assignment may be inconsistent with system definitions. A correct assignment may be incorrectly specified to the system generator or incorrectly implemented by switch settings or jumper placements.

1. Using Sections 3.5 and 3.6, verify that address and vector assignments and switch settings are correct.

2. Using Section 3.9, check that interrupt priority jumpers are correctly placed and are making contact.

3. Using Section 3.10, verify that the wire between pins CA1 and CB1 of a DEC DH/DM backplane slot has been removed.

4. If the problem involves 200 baud or external B speed selections, use Section 3.7 to check that the correct baud range is selected.

5. Use a voltmeter to verify that the +5V, +15V, and -15V are within +5% of their nominal value. If not, adjust the associated power supplies. See Table 4-1 for the backplane pins at which these voltages appear.

Voltage	Backplane Pins
+5V	AA2, BA2, CA2, DA2, EA2, FA2
+15V	CU1
-15V	CB2, DB2, EB2, FB2
Ground	AC2, BC2, CC2, CD2, EC2, FC2

Table 4-1: Voltage Sources on Backplane

Once you are certain that DH/DM is correctly configured and installed and is receiving appropriate input power, DEC diagnostic ZDHM can be used to assign trouble between the DH/DM and external equipment or cabling.

It should be noted that this diagnostic will detect a speed error unless the external B frequency is set for 200 baud.

If a fault in a DH/DM board is indicated, call ABLE as described in Sections 4.3 and 4.4.

4.2.3 FAILS ZDHM DIAGNOSTIC

If an error is reported when running the ZDHM diagnostic, we suggest you take the following steps:

1. Verify that none of the DH/DM LEDs are lit.

2. Verify that the cables are installed in the maintenance connectors (J7 and J8) on the EIA panel.

3. Remove the DH/DM board and re-verify that the desired address and vector assignments are set correctly.

4. Re-install the board and run the diagnostic again.

If the error persists, please contact the ABLE Product Support Center as described in Sections 4.3 and 4.4.

4.2.4 FAILS SYSTEM SOFTWARE

If the DH/DM is suspected of causing failures within the system software, we request that you run a diagnostic to determine whether the DH/DM unit is good or bad. If the DH/DM operates the diagnostic properly and only fails the system software, check the address and vector assignments to ensure that they conform to SYSGEN parameters.

If the failure persists, contact the ABLE Product Support Center as described in Sections 4.3 and 4.4.

4.3 WHO TO CALL FOR SERVICE WITHIN THE UNITED STATES

ABLE's goal is to provide each customer with a product that works well in his system. We design and build our products to provide high reliability and to minimize problems. When a problem does arise, it is our intent to do everything in our power to quickly and efficiently solve it.

If your DH/DM does not function properly and you are within the United States, contact our Product Support Center before sending it for repair: (Have serial numbers available when calling.)

ABLE COMPUTER
1732 Reynolds Avenue
Irvine, California 92714
(714) 979-7030
TWX 910-595-1729

If your DH/DM requires repair, we prefer that you return it to the factory.

When shipping the DH/DM use the original container or a corregated cardboard carton with at least one inch of cushioning material on all sides. Ship it to the above address. Include a description of the problem and a hard copy of the failure mode or a diagnostic printout when available. Be sure to include your name, address, and telephone number.

4.4 WHO TO CALL FOR SERVICE OUTSIDE THE UNITED STATES

ABLE's goal is to provide each customer with a product that works well in his system. We design and build our products to provide high reliability and to minimize problems. When a problem does arise, it is our intent to do everything in our power to quickly and efficiently solve it.

If your DH/DM does not function properly, contact your local distributor or telex ABLE COMPUTER for the name and address of your local distributor:

TWX 910-595-1729

SECTION 5
HOW TO USE DH/DM

5.1 TYPICAL APPLICATIONS

The DH/DM connects a PDP-11 or VAX system to sixteen terminals designed to interface with asynchronous communications lines. It provides direct memory access (DMA) ouput capabilities.

Figure 5-1 illustrates typical interfaces between the DH/DM and local or remote terminals.

The DH/DM is used to interface with local terminal devices or, via modems and dedicated lines, with remote terminal devices. When commumicating with remote terminals via datasets interfacing over switched networks, modem control is available for all lines.

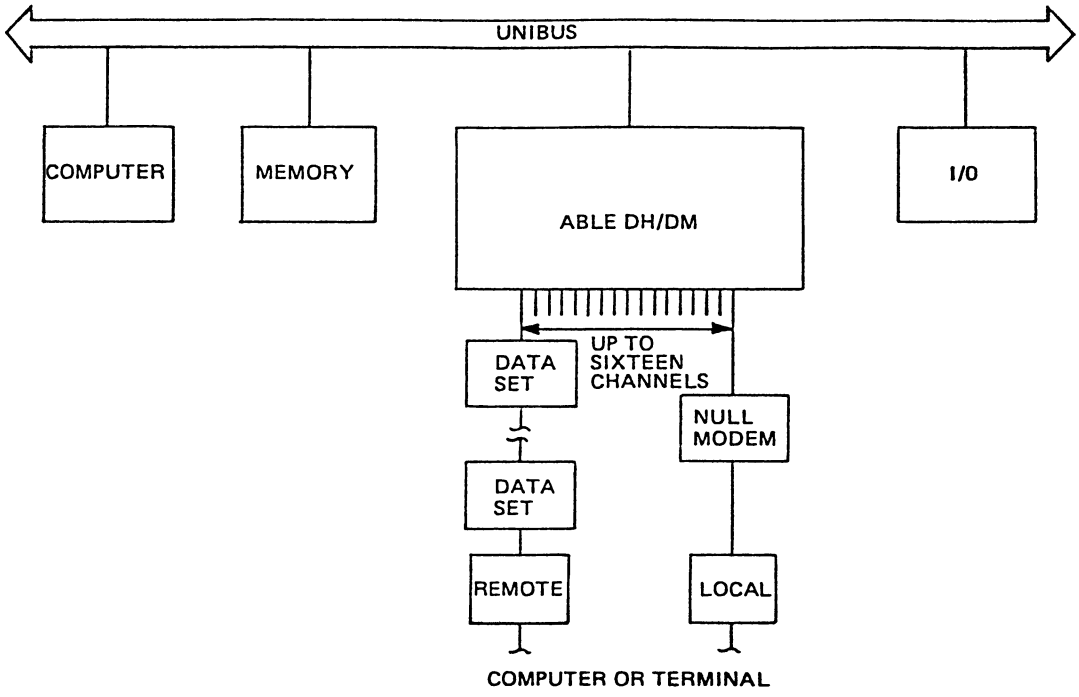

Figure 5-1: DH/DM Applications

5.2 TERMINAL/COMMUNCATIONS LINK INTERFACE INFORMATION

Table 5-1 lists the pin assignments on connectors J1 and J2 on the DH/DM. These connectors provide the interface with the external distribution system for a DH/DM.

Table 5-2 lists pin assignments for the EIA RS232-C connectors on the EIA distribution panel. Notice that certain internal lines are hard-wired to connector pins and others are connected through jumpers installed on the EIA distribution panel. Jumper placements have been selected to provide compatibility with the greatest possible number of modem interfaces. Modifications to jumper placements may be required for certain interfaces. Figure 5-2 shows the location of the jumpers on the panel. Figure 5-3 provides wiring information for modem connection.

5.3 UNIBUS CONNECTOR INFORMATION

Table 5-3 lists the Unibus signals accepted or supplied by the DH/DM via the connectors on the board.

	J1		
DTR00-H	1	2	CARR00-H
DTR01-H	3	4	CARR01-H
DTR02-H	5	6	CARR02-H
DTR03-H	7	8	CARR03-H
DTR04-H	9	10	CARR04-H
DTR05-H	11	12	CARR05-H
DTR06-H	13	14	CARR06-H
DTR07-H	15	16	CARR07-H
GND	17	18	GND
TXD00-H	19	20	RING00-H
RXD00-H	21	22	GND
TXD01-H	23	24	RING01-H
RXD01-H	25	26	GND
TXD02-H	27	28	RING02-H
RXD02-H	29	30	GND
TXD03-H	31	32	RING03-H
RXD03-H	33	34	GND
TXD04-H	35	36	RING04-H
RXD04-H	37	38	GND
TXD05-H	39	40	RING05-H
RXD05-H	41	42	GND
TXD06-H	43	44	RING06-H
RXD06-H	45	46	GND
TXD07-H	47	48	RING07-H
RXD07-H	49	50	GND

	J2		
DTR08-H	1	2	CARR08-H
DTR09-H	3	4	CARR09-H
DTR10-H	5	6	CARR10-H
DTR11-H	7	8	CARR11-H
DTR12-H	9	10	CARR12-H
DTR13-H	11	12	CARR13-H
DTR14-H	13	14	CARR14-H
DTR15-H	15	16	CARR15-H
GND	17	18	GND
TXD08-H	19	20	RING08-H
RXD08-H	21	22	GND
TXD09-H	23	24	RING09-H
RXD09-H	25	26	GND
TXD10-H	27	28	RING10-H
RXD10-H	29	30	GND
TXD11-H	31	32	RING11-H
RXD11-H	33	34	GND
TXD12-H	35	36	RING12-H
RXD12-H	37	38	GND
TXD13-H	39	40	RING13-H
RXD13-H	41	42	GND
TXD14-H	43	44	RING14-H
RXD14-H	45	46	GND
TXD15-H	47	48	RING15-H
RXD15-H	49	50	GND

Table 5-1: Connectors on DH/DM Board

PIN NUMBER	DESIGNATION	CIRCUIT DESCRITPION	HARD-WIRED	JUMPER-WIRED
1	AA	Protective Ground	GND	
2	BA	Transmitted Data	TXDn-H	
3	BB	Received Data	RXDn-H	
4	CA	Request To Send		RTSn-H
5	CB	Clear To Send	CTSn-H	
6		Unassigned		
7	AB	Signal Ground (Common Return)	GND	
8	CF	Received Line Signal Detector	CARRn-H	
9		Unassigned		
10		Unassigned		
11	SBA	Secondary Transmitted Data	STXn-H	
12	SBB	Secondary Received Data	SRXn-H	
13		Unassigned		
14	SBA	Secondary Transmitted Data		STXn-H
15		Unassigned		
16	SBB	Secondary Received Data		SRXn-H
17	SBB	Secondary Received Data		SRXn-H
18		Unassigned		
19		Unassigned		
20	CD	Data Terminal Ready	DTRn-H	
21		Unassigned		
22	CE	Ring Indicator	RINGn-H	
23		Unassigned		
24	CA	Request To Send		RTSn-H
25		Unassigned		

n = Channel Number

Table 5-2: RS232-C Connector Pin Assignments

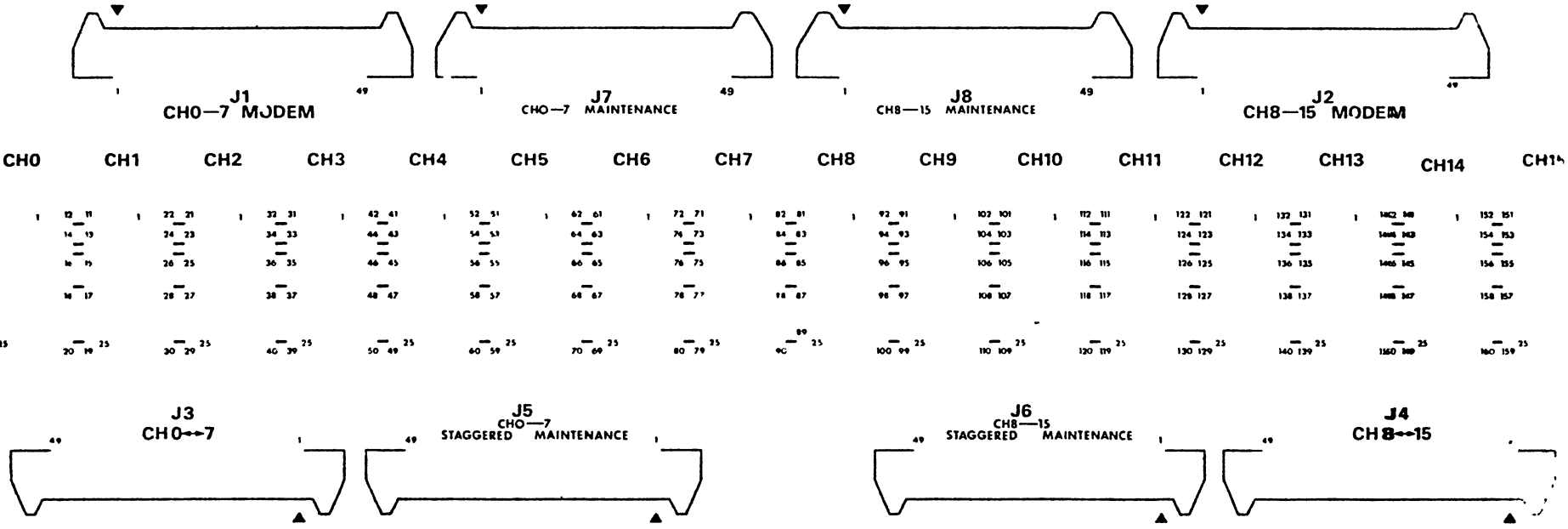

Figure 5-2: Jumper Terminal Locations, EIA Distribution Panel

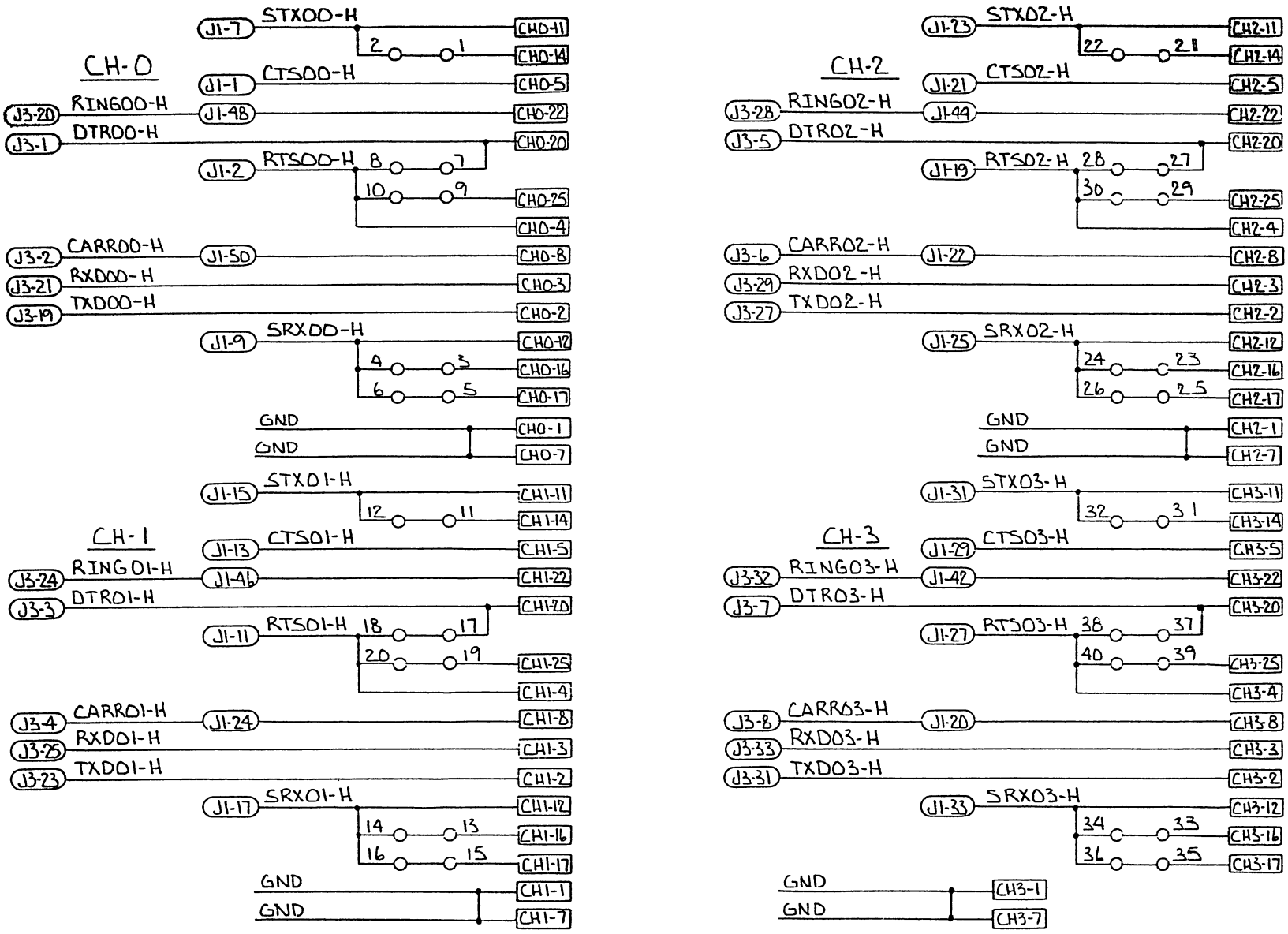

Figure 5-3: Wiring Chart For Modem Connection

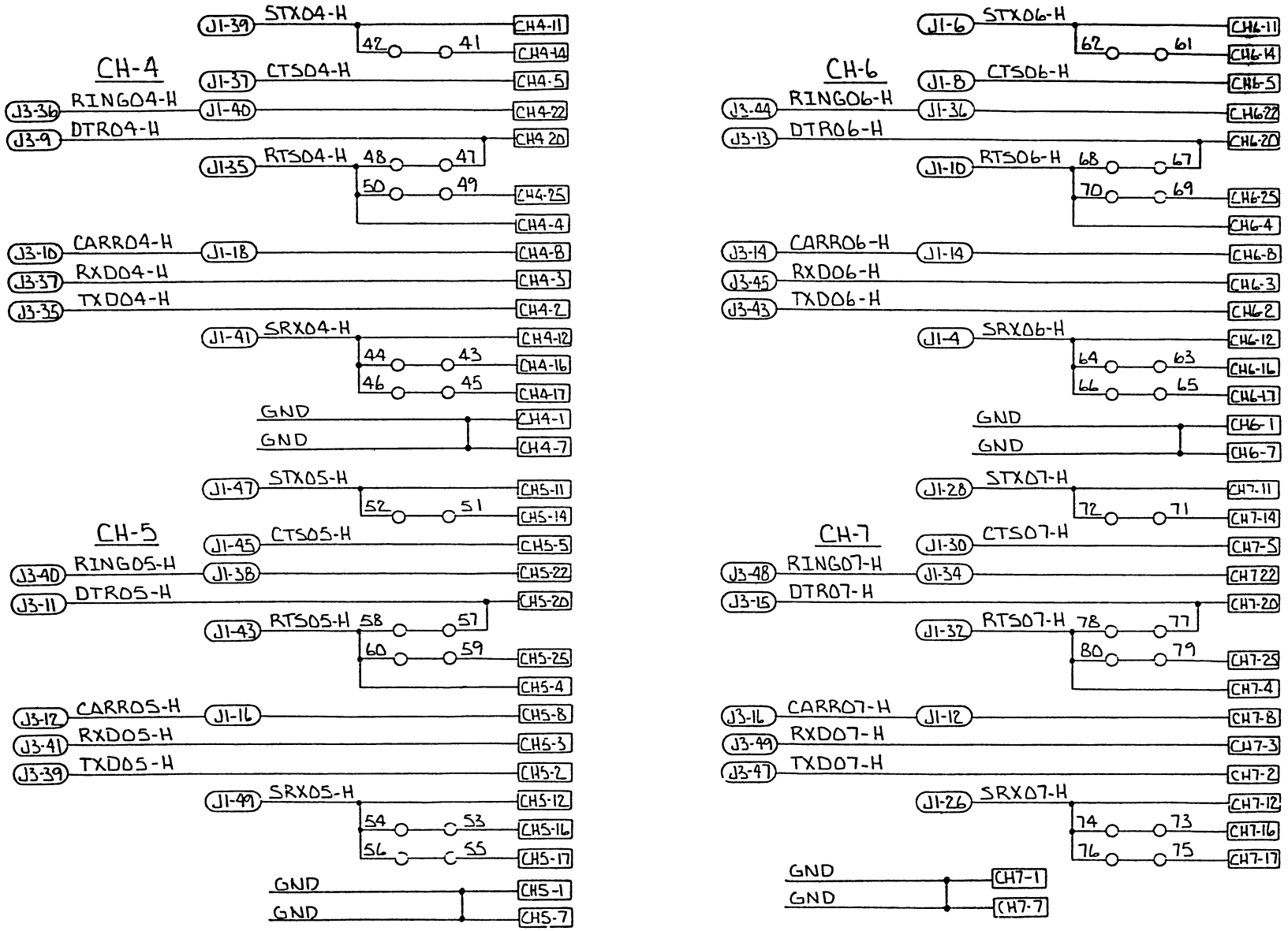

Figure 5-3: Wiring Chart For Modem Connection (Con't.)

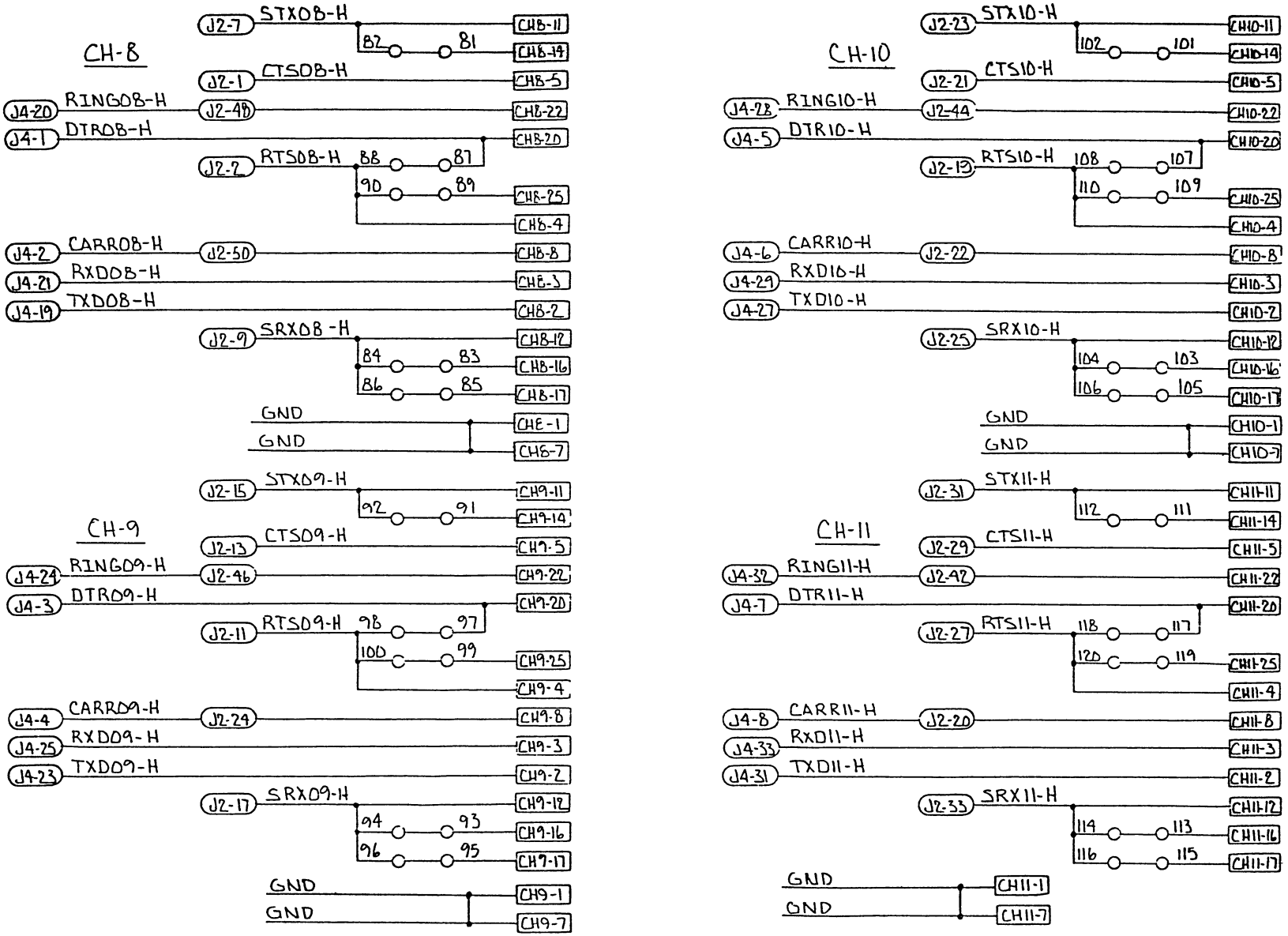

Figure 5-3: Wiring Chart For Modem Connection (Con't.)

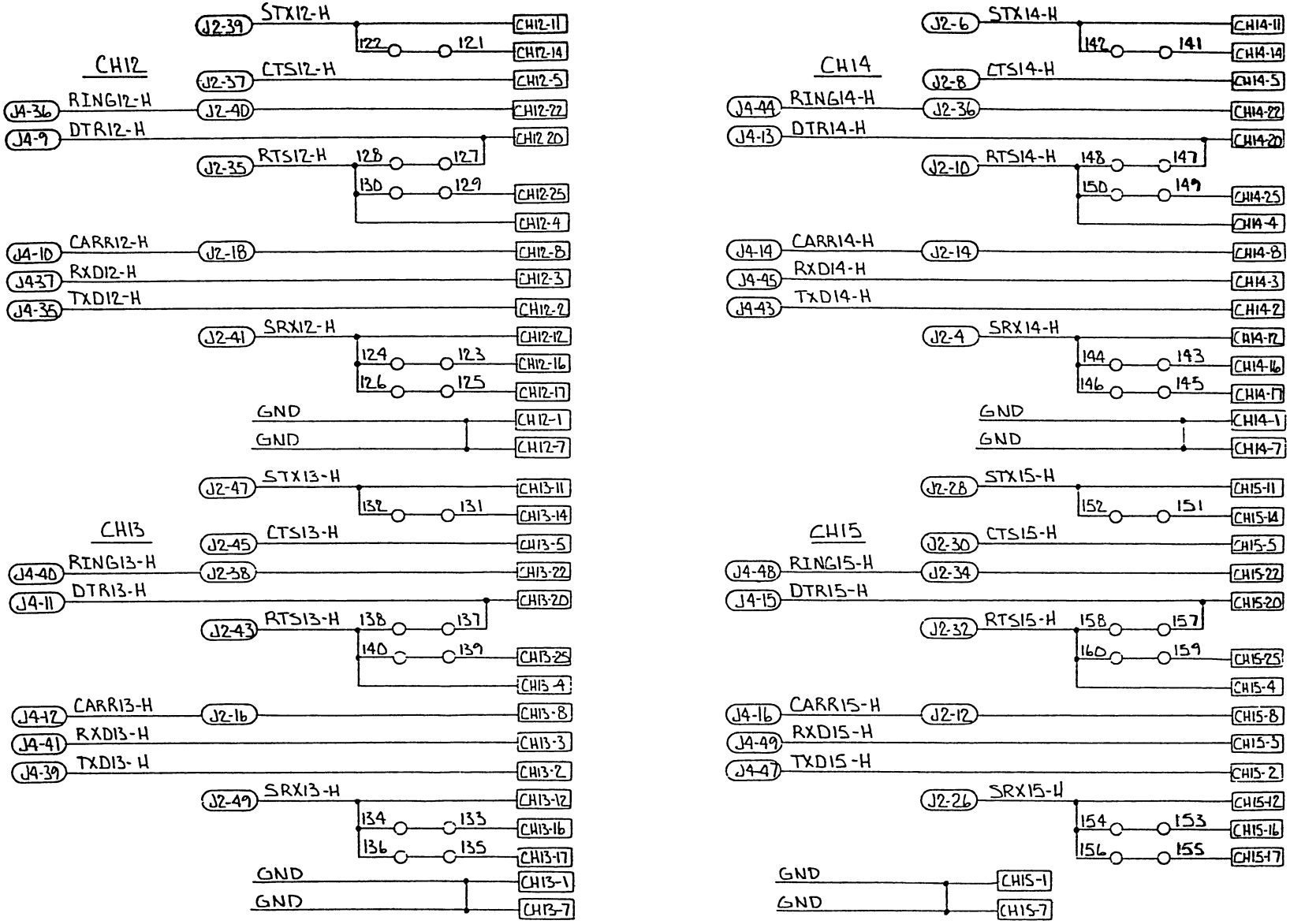

Figure 5-3: Wiring Chart For Modem Connection (Con't.)

CONNECTOR A		
SIDE 1	PIN	SIDE 2
	A	+5V
	B	
	C	GND
	D	
	E	
	F	
	H	
	J	
	K	
	L	
	M	
BUS-A21-L	N	
BUS-A20-L	P	
	R	
	S	
GND	T	
	U	
	V	

CONNECTOR B		
SIDE 1	PIN	SIDE 2
	A	+5V
	B	
	C	GND
	D	
BUS-A19-L	E	BUS-A18-L
	F	
	H	
	J	
	K	
	L	
	M	
	N	
	P	
	R	
	S	
GND	T	
	U	
	V	

CONNECTOR C		
SIDE 1	PIN	SIDE 2
BUS-NPG-IN-H	A	+5V
BUS-NPGO-H	B	-15V
	C	GND
	D	BUS-D15-L
	E	BUS-D14-L
	F	BUS-D13-L
BUS-D11-L	H	BUS-D12-L
	J	BUS-D10-L
	K	BUS-D09-L
	L	BUS-D08-L
	M	BUS-D07-L
BUS-DCLO-L	N	BUS-D04-L
	P	BUS-D05-L
	R	BUS-D01-L
BUS-PB-L	S	BUS-D00-L
GND	T	BUS-D03-L
+15V	U	BUS-D02-L
	V	BUS-D06-L

CONNECTOR D		
SIDE 1	PIN	SIDE 2
	A	+5V
	B	
	C	GND
	D	BUS-BR7-L
	E	BUS-BR6-L
	F	BUS-BR5-L
	H	BUS-BR4-L
	J	
	K	BUS-BG7-IN-H
BUS-INIT-L	L	BUS-BG7-OUT-H
	M	BUS-BG6-IN-H
	N	BUS-BG6-OUT-H
	P	BUS-BG5-IN-H
	R	BUS-BG5-OUT-H
	S	BUS-BG4-IN-H
GND	T	BUS-BG4-OUT-H
	U	
	V	

Table 5-3. DH/DM Board Interface with Unibus Connectors A Through F

CONNECTOR E		
SIDE 1	PIN	SIDE 2
	A	+5V
	B	
BUS-A12-L	C	GND
BUS-A17-L	D	BUS-A15-L
BUS-MSYN-L	E	BUS-A16-L
BUS-A02-L	F	BUS-C1-L
BUS-A01-L	H	BUS-A00-L
BUS-SSYN-L	J	BUS-C0-L
BUS-A14-L	K	BUS-A13-L
BUS-A11-L	L	
	M	BUS-A08-L
	N	BUS-A07-L
BUS-A10-L	P	
BUS-A09-L	R	
	S	
GND	T	
BUS-A06-L	U	BUS-A04-L
BUS-A05-L	V	BUS-A03-L

CONNECTOR F		
SIDE 1	PIN	SIDE 2
	A	+5V
	B	
	C	GND
BUS-BBSY-H	D	
	E	
	F	
	H	
BUS-NPR-L	J	
	K	
	L	
BUS- INTR-L	M	
	N	
	P	
	R	
	S	
GND	T	BUS-SACK-L
	U	
	V	

Table 5-3: DH/DM Board Interface with Unibus Connectors A Through F (Con't.)

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SECTION 6
HOW TO PROGRAM DH/DM

6.1 DATA HANDLING REGISTERS

The data handling portion of the DH/DM is software compatible with the DEC DH11. It contains eight Unibus addressable registers. Table 6-1 contains general information about these registers. As illustrated in Figure 6-1, three of these are actually 16-register groups with one register for each line. When one of these register groups is addressed, the particular register within the group that is selected is determined by the line number currently held in the four least significant bit positions of the system control register (SCR). Figure 6-2 illustrates register format.

The following paragraphs describe the function of each register.

Register	Address	Access	Word/Byte Addressable
System Control Register	X00	Mixed See 6.1.1	Word/Byte
Next Received Character Register	X02	Read Only	Word Only
Line Parameter Register (Group)	X04	Read/Write	Word Only
Current Address Register	X06	Read/Write	Word Only
Byte Count Register (Group)	X10	Read/Write	Word Only
Buffer Active Register	X12	Read/Write	Word Only
Break Control Register	X14	Read/Write	Word/Only
Silo Status Register	X16	Mixed See 6.1.8	Word/Byte

Table 6-1: Data Handling Register List

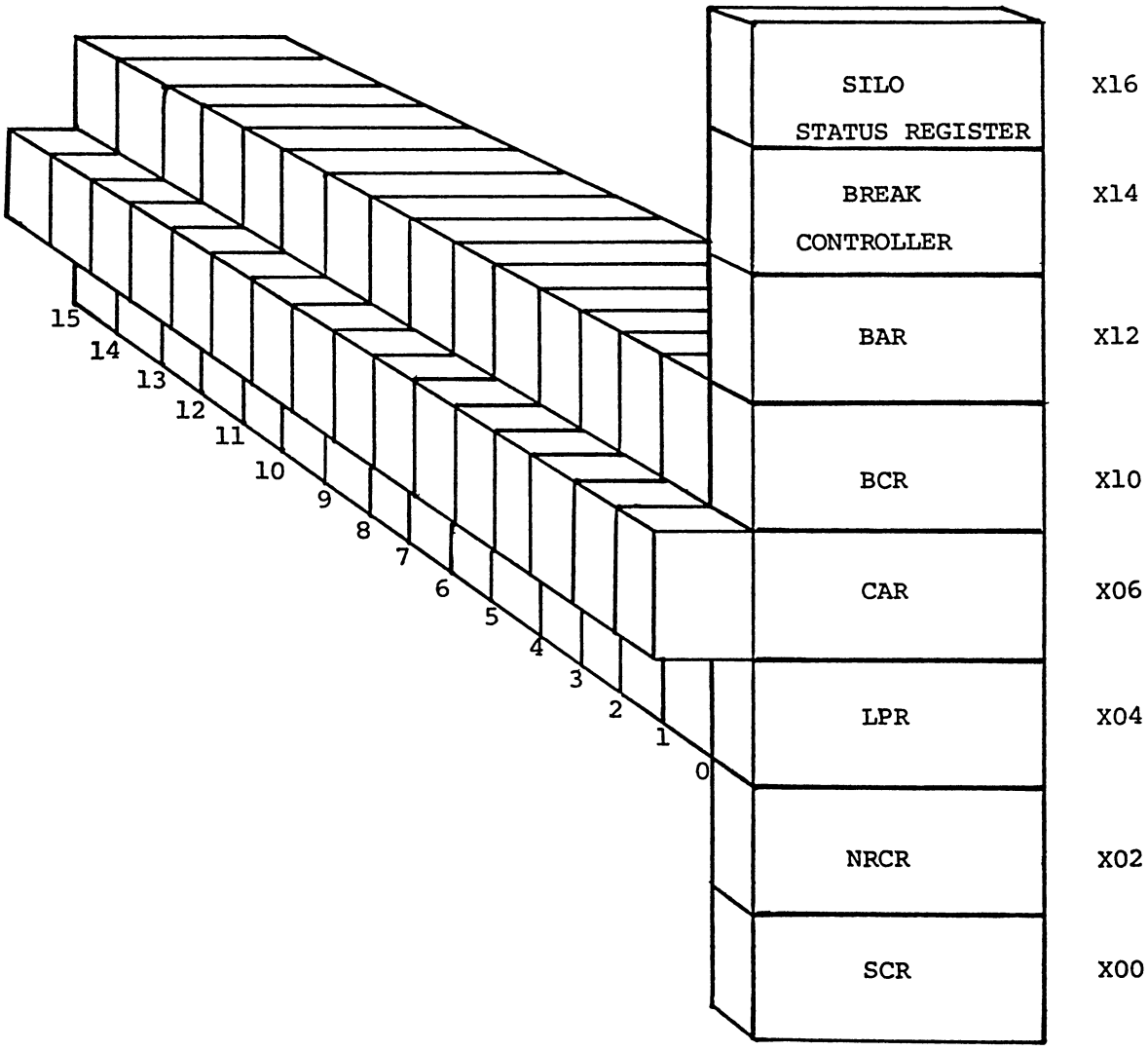
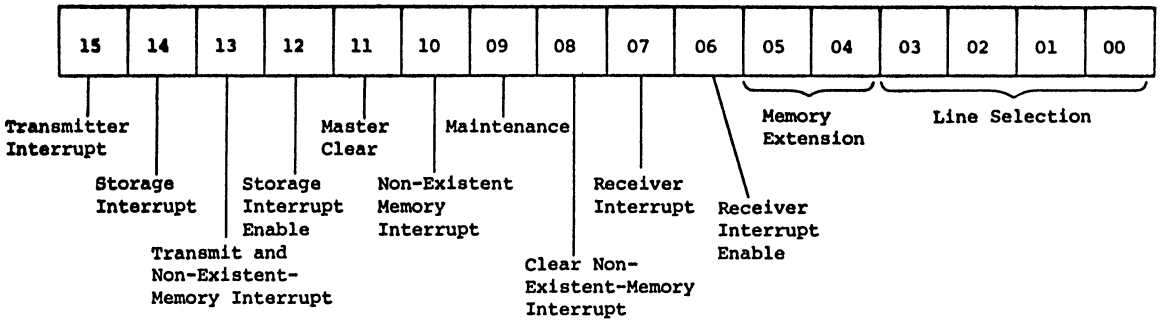
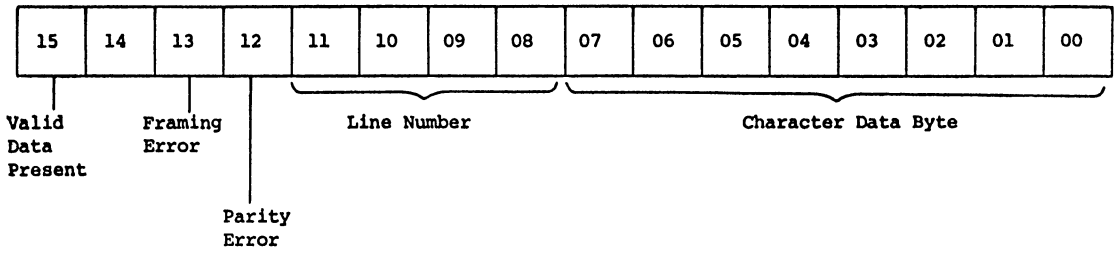


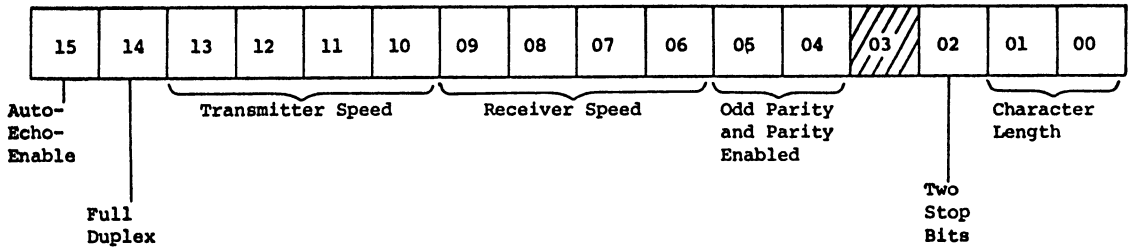
Figure 6-1: Data Handling Registers



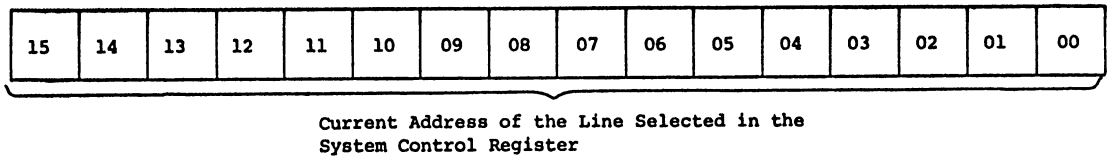
SYSTEM CONTROL REGISTER (X00) (See Section 6.1.1)



NEXT RECEIVED CHARACTER REGISTER (X02) (See Section 6.1.2)

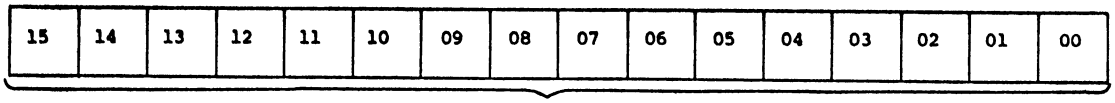


LINE PARAMETER REGISTER (X04) (See Section 6.1.3)

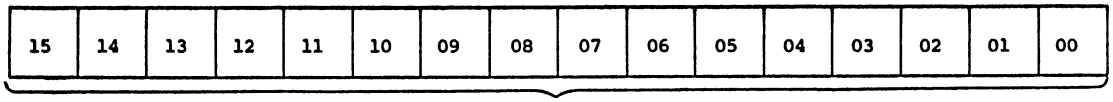


CURRENT ADDRESS REGISTER (X06) (See Section 6.1.4)

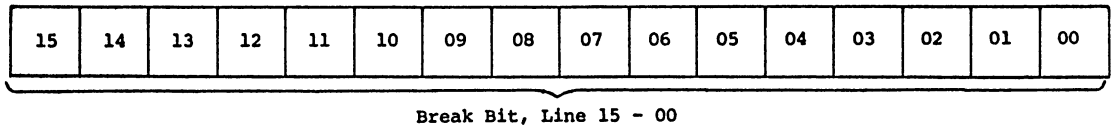
Figure 6-2: Data Handling Register Formats



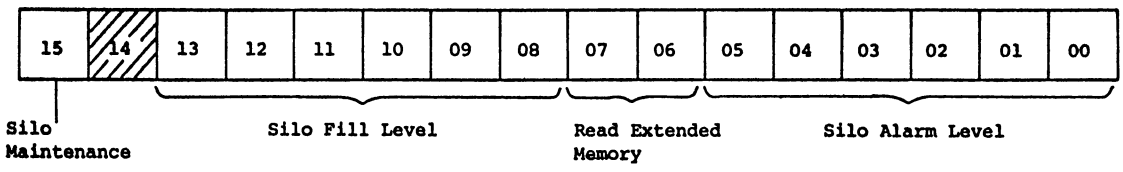
BYTE COUNT REGISTER (X10) (See Section 6.1.5)



BUFFER ACTIVE REGISTER (X12) (See Section 6.1.6)



BREAK CONTROL REGISTER (X14) (See Section 6.1.7)



SILO STATUS REGISTER (X16) (See Section 6.1.8)

Figure 6-2: Data Handling Register Formats

(Con't.)

6.1.1 SYSTEM CONTROL REGISTER

Bit	Description
15	Transmitter Interrupt. This read/write bit is set when the final character in a message buffer is loaded into a UART transmitter holding register. It causes an interrupt if bit 13 is set.
14	Storage Interrupt. This bit is set when a character transfer from a receiver holding register to the silo is inhibited because the silo is full. It causes an interrupt if bit 12 is set. This bit is read only in the normal mode and read/write in the maintenance mode. When not in the maintenance mode, the silo has a 255 character capacity.
13	Transmit and Non-Existent-Memory Interrupt Enable. When set, this read/write bit enables an interrupt in response to the setting of bit 10 or bit 15.
12	Storage Interrupt Enable. When set, this read/write bit enables an interrupt in response to the setting of bit 14.
11	Master Clear. When set, this read/write bit places the data handling portion of the DH/DM in the initialized status in which the silo, the UARTs, and most register bits are cleared.
10	Non-Existent-Memory Interrupt. This bit is set if no slave sync response is received within 20 microseconds of the assertion of master sync by the DH/DM during an NPR transaction. The lack of response indicates that the addressed memory location does not exist. Setting this bit causes an interrupt if bit 13 is set. This bit is read only in the normal mode and read/write in the maintenance mode.
09	Maintenance. When set, this read/write bit places the DH/DM in the maintenance mode.
08	Clear Non-Existent-Memory Interrupt. When set, this bit clears bit 10 and itself.
07	Receiver Interrupt. This bit is set when the number of characters stored in the silo exceeds the alarm level specified by the low byte of the silo status register. It generates an interrupt if bit 06 is set. This bit is read only in the normal mode and is read/write in the maintenance mode. If there are fewer than sixteen characters in the silo, there may be a delay of up to 20ms before setting this bit. This reduces interrupt overhead.
06	Receiver Interrupt Enable. When set, this read/write bit enables an interrupt in response to the setting of bit 07.

Bit	Description
05, 04	Memory Extension. When the program writes the current address register for the line selected by bits 03 through 00, read/write bits 05 and 04 are written into bits 17 and 16 of that current address register. When the system control register is read, the bit 05 and 04 values are those most recently written into these bit positions. Notice that these are not necessarily the current values of bits 17 and 16 of the current address register for the currently selected line.
03 - 00	Line Selection. These read/write bits specify the line (horizontal) address of the register to be written or read when the line-parameter, current address, or byte count register is addressed.

6.1.2 NEXT RECEIVED CHARACTER REGISTER (X02)

Bit	Description
15	Valid Data Present. This bit is set when the remaining bit positions of the register contain valid information and is reset when the register is empty.
14	Data Overrun. This bit is set when at least one preceding character of the same message has been overwritten and lost in the UART holding register.
13	Framing Error. This bit is set when the current character was not framed by the programmed number of stop bits. This is usually interpreted as the reception of a break.
12	Parity Error. This bit is set when the current character exhibited incorrect parity as received from the line.
11 - 8	Line Number. These bits contain the number of the line from which the character was received.
07 - 00	Character Data Byte. This byte contains the data bits of a character from the line whose number appears in bits 11 through 08. When the character has less than eight data bits, these bits are right-justified and unused bits of the byte are zeros.

6.1.3 LINE PARAMETER REGISTER (X04)

Prior to transmitting or receiving messages on a line, the program must define certain parameters for the line by writing the line parameter register. In order to write into the line parameter register for a line,

That line number must first be written into the system control register. The line parameter register is a read/write operation register, but when read it reflects the value last written, and not the value for the currently selected line.

Bit	Description
15	Auto-Echo-Enable. When this bit is set, characters received on the line are automatically transmitted back (echoed) on the line by DH/DM.
14	Half/Full Duplex. In the full duplex mode (bit 14=0), transmission and reception can occur simultaneously. In half duplex mode (bit 14=1), the receiver is disabled when characters are being transmitted.
13 - 10	Transmitter Speed. These bits define the transmitter baud rate as summarized in the table below.

13	12	11	10	Speed (Baud)	13	12	11	10	Speed (Baud)
0	0	0	0	Zero	1	0	0	0	600
0	0	0	1	50	1	0	0	1	1200
0	0	1	0	75	1	0	1	0	1800
0	0	1	1	110	1	0	1	1	2400
0	1	0	0	134.5	1	1	0	0	4800
0	1	0	1	150	1	1	0	1	9600
0	1	1	0	200	1	1	1	0	19200
0	1	1	1	300	1	1	1	1	External

Note: There are the following two restrictions associated with speed selection:

1. The 200 and External rates are actually obtained from a common clock on the DH/DM. Thus, if this clock is set for the 200 baud rate, that also becomes the external rate. Conversely, if that clock is set for some other external rate, then the 200 baud rate is unavailable.

2. Different receiver and transmitter speeds can be selected for or a given line if only one of these is zero or obtained from the clock shared by the External and 200 selection values.

09 - 06 Receiver Speed. These bits define the receiver bit rate in the same manner and with the same restrictions that bits 13 - 10 define the transmitter baud rate.

Bit	Description

05, 04 — Odd Parity and Parity Enabled. The combined states of these bits determine the parity generated by the UART transmitter and the parity required by the UART receiver for the line as follows:

05	04	Parity
0	0	None
0	1	Even
1	0	None
1	1	Odd

03 — Not used.

02 — Two Stop Bits. When this bit is set, 1.5 stop bits are appended to transmitted characters having 5 data bits and 2 stop bits are appended transmitted characters having from 6 through 8 data bits. When this bit is reset, one stop bit is appended to all transmitted characters regardless of length.

Note: Unlike some asynchronous receivers, the DH/DM receiver can be programmed to receive one or two stop bits. When two stop bits are specified, the receiver checks for two stop bits. Data that is received with only one stop bit can cause receiver errors. To ensure error-free operation, set this field as it would normally be set--with the number of stop bits for the DH/DM receiver matching the number of stop bits in the received data.

01, 00 — Character Length. These two bits specify the number of data bits in received and transmitted characters as follows:

01	00	Data Bits
0	0	5
0	1	6
1	0	7
1	1	8

6.1.4 CURRENT ADDRESS REGISTER (X06)

Prior to transmitting a message over a line, the program must write the starting address of the data buffer containing the message into the current address register for that line. This involves first writing the line number and the address extension bits into the system control register and then transferring the remainder of the starting address directly to the current address register. During this second transfer, Unibus bits 00 through 15 are written into bit positions 00 through 15 of the current address register and the address extension bits from bit positions 04 and 05 of the system control register are written into bit positions 16 and 17 of the current address register.

To read the current address for a line, the program must write the line number into the system control register. It can then read bits 00 through 15 of the current address by reading the current address register and bits 16 through 17 by reading the silo status register which contains these bits in bit positions 06 and 07.

6.1.5 BYTE COUNT REGISTER (X10)

Prior to transmitting a message over a line, the program must also write the 2's complement of the number of characters (bytes) in the message into the byte count register. As in the case of the line parameter and current address register, the line number must first be written into the system control register in order to address the byte count register for the line. The byte count register can then be either written or read by the program.

6.1.6 BUFFER ACTIVE REGISTER (X12)

This register contains one bit for each line; where bit n is the bit for line n. The program sets bit n to start transmission of a message over line n after the message has been written in a data buffer in PDP-11 memory and the starting address and length of the data buffer have been transferred to the current address register and byte count register for the line. The DH/DM subsequently resets the bit for the line at the time that the last character of the message is loaded into the UART holding register. Because the DH/DM resets the bits in this register, the program must use BIS instructions to set these bits.

6.1.7 BREAK CONTROL REGISTER (X14)

This register contains one bit for each line; where bit n is the bit for line n. The program sets the bit for a line to start the transmission of a break on that line and resets the bit to terminate the transmission of the break. (Refer to paragraph 6.4 for break control timing information.)

6.1.8 SILO STATUS REGISTER (X16)

Bit	Description
15	Silo Maintenance. When set, this read/write bit causes a fixed binary pattern to be sent to the silo for checking.
14	Not used.
13 - 08	Silo Fill Level. These read-only bits indicate the number of characters currently held in the silo. 000000 can indicate either an empty silo or a silo with more than 63 characters. For an empty silo, the valid data present bit (15) of the next received character register is reset while for a silo with more than 63 characters, it is set. Also if an attempt has been

Bit	Description
	made to load another character into a full silo, then the storage overflow bit (14) of the system control register is set.
07, 06	Read Extended Memory. These read-only bits are A17 and A16 of the current address register for the line whose number is held in the line selection field (bits 03 through 00) of the system control register.
05 - 00	Silo Alarm Level. When the silo fill level exceeds the value written into this read/write field by the program, receiver interrupt bit 07 of the system control register is set. If receiver interrupt enable bit 06 of the system control register is set, this causes an interrupt. If there are fewer than sixteen characters in the silo, there may be a delay of up to 20ms before setting this bit. This reduces interrupt overhead. NOTE: Switch 4-3 controls the 20 MS silo alarm delay. Reference Section 3.7.2.

6.2 MODEM REGISTERS

The DM portion implements a software compatible subset of the DEC DM11-BB. It contains two Unibus addressable registers, the control and status register and the line status register. As illustrated in Figure 6-3, the byte-wide line status register is actually a register group that includes one register for each line. When the line status register group is addressed, the particular register is read or written as determined by the line number held in the control and status register. The following paragraphs describe the two registers. Figure 6-4 illustrates register formats.

Note: The only actual signals are Ring, Carrier, and Data Terminal Ready. All others exist for software compatibility.

6.2.1 CONTROL AND STATUS REGISTER

Bit	Description
15	Ring Flag. This read-only bit and DONE (bit 7) are set when a transition from OFF to ON is detected for the RING signal from the line specified by bits 3 through 0. Setting CLEAR SCAN (bit 11) resets the stored value of RING so that an existing ON condition appears as a transition and sets this bit and DONE.
14	Carrier Flag. This read-only bit and DONE (bit 7) are set when any transition of the CARRIER signal from the line specified by bits 3 through 0 is detected. Setting CLEAR SCAN (bit 11) resets the stored value of CARRIER so that an

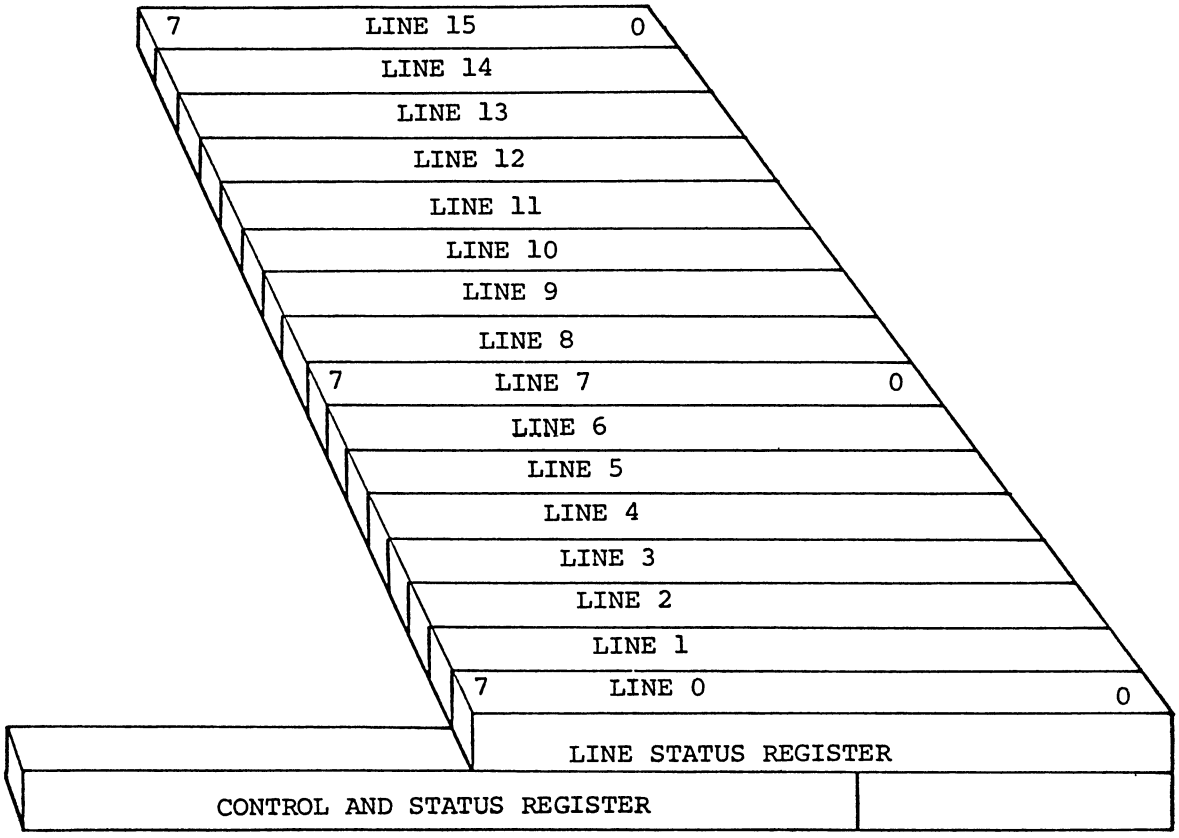
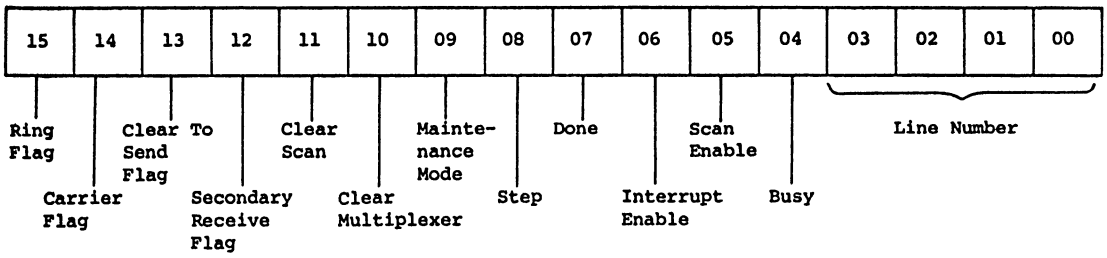
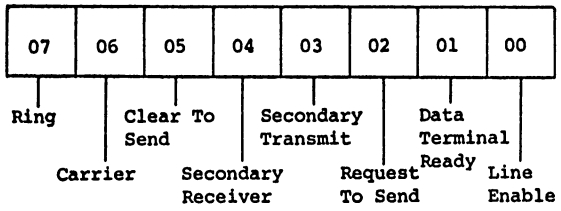


Figure 6-3: Modem Registers



CONTROL AND STATUS REGISTER (770XX0) (See Section 6.2.1)



LINE STATUS REGISTER (770XX2) (See Section 6.2.2)

Figure 6-4: Modem Register Formats

Bit	Description
	existing ON condition appears as a transition and sets this bit and DONE.
13	Clear to Send Flag. This read-only bit and DONE (bit 7) are set when any transition of the CLEAR TO SEND signal from the line specified by bits 3 through 0 is detected. Setting CLEAR SCAN (bit 11) resets the stored value of CLEAR TO SEND so that an existing ON condition appears as a transition and sets this bit and DONE.
12	Secondary Receive Flag. This read-only bit and DONE (bit 7) are set when any transition of the SECONDARY RECEIVE signal from the line specified by bits 3 through 0 is detected. Setting CLEAR TO SCAN (bit 11) resets the stored value of SECONDARY RECEIVE so that an existing ON condition appears as a transition and sets this bit and the DONE bit.
11	Clear Scan. Writing a ONE into this write-ONE-only bit generates a pulse which clears bits 9, 7, 6, 5, and 3 through 0 and initiates a sequence which clears the scan memory. With the scan memory cleared, any ON condition of a RING, CARRIER, CLEAR-TO-SEND, or SECONDARY RECEIVE signal is detected as a change of state during subsequent scanning and causes the associated change flag (bits 15 through 12) to set.
10	Clear Multiplexer. Writing a ONE into this write-ONE-only bit generates a pulse which clears bits 3 through 0 (SECONDARY TRANSMIT, REQUEST TO SEND, DATA TERMINAL READY, LINE ENABLE) of all 16 line status registers.
09	Maintenance Mode. Setting this read/write bit forces the RING, CARRIER, CLEAR TO SEND, and SECONDARY RECEIVE inputs to the line scanner to the ON condition for test purposes. If this is preceded by the writing of a ONE into CLEAR SCAN (bit 11) then an interrupt (if enabled) should be generated for every line that is scanned.
08	Step. Each time that a ONE is written into this write-ONE-only bit, a STEP sequence having a duration of 1 μsec ±10% is initiated. During this sequence, the line number held in bits 3 through 0 is incremented, signals from the newly addressed line are evaluated for transitions, and change flags (bits 15 through 12) and the DONE flag (bit 7) are set if any transitions are detected. This bit can be used rather than SCAN ENABLE (bit 5) to provide a scan rate controlled by the program. Note, however, that this scan rate should be high enough so that CARRIER signals will not switch ON and OFF during the interval between successive

Bit	Description
	scans of a line. Note also that DONE does not inhibit STEP.
07	Done. This read/write bit is set when bit 15, 14, 13, or 12 sets. With DONE set, the line scanner is disabled so that bits 3 through 0 continue to contain the number of the line associated with the condition which causes DONE to set. If INTERRUPT ENABLE bit 6 is also set, an interrupt normally resets DONE so as to release the line scanner. This bit is also reset by INITIALIZE and by CLEAR SCAN (bit 11).
06	Interrupt Enable. When this read/write bit is set, the DM interrupt function is enabled. The bit is cleared by INITIALIZE and by CLEAR SCAN (bit 11).
05	Scan Enable. When this read/write bit is set the DM is placed in the automatic scanning mode. In this mode, the scanner increments the line number held in bits 03 through 00 and checks for transitions of the signals from the newly addressed line at a rate of approximately 1 microsecond per line until a transition is found. At this time the appropriate transition flag (bits 15 through 12) and DONE (bit 07) are set. Scanning is then inhibited until the program resets the DONE bit.
04	Busy. This read-only bit is set when lines are being scanned. Program should change line number (bits 03 through 0) only when BUSY is 0.
03 - 00	Line Number. These read/write bits, held in a counter, point to one of the 16 line-status registers and select inputs from one of the 16 lines for transition detection. The line number is incremented at the start of each scan cycle and is reset to 0000 by INITIALIZE or by CLEAR SCAN (bit 11). Notice, that since the incrementing of the count occurs at the start of each scan cycle, the first line tested after a reset is 0001 rather than 0000.

6.2.2 LINE STATUS REGISTER

Bit	Description
07	Ring. This read-only bit indicates the status of the modem RING signal.
06	Carrier. This read-only bit indicates the status of the modem CARRIER signal.

Bit	Description
05	Clear to Send. This read-only bit indicates the status of the modem CARRIER signal.
04	Secondary Receive. This read-only bit indicates the status of the modem SECONDARY RECEIVE signal.
03	Secondary Transmit. When set, this read/write bit presents a MARK to the SECONDARY TRANSMIT input of the modem. This bit is reset by INITIALIZE or by CLEAR MUX (bit 10) of the control and status register.
02	Request to Send. This is used to condition the modem to transmit if all other conditions are met. The bit is cleared by INITIALIZE and CLEAR MUX. It is Read/Write.
01	Data Terminal Ready. This bit allows the modem to enter and maintain the data mode. It is cleared by INITIALIZE and CLEAR MUX. This bit is Read/Write.
00	Line Enable. This bit enables the state of RING, CARRIER, CLEAR TO SEND, and Sec Rx to be sampled by the program and tested for transitions. It is cleared by INITIALIZE and CLEAR MUX. This bit is Read/Write.

6.3 TRANSMITTER/RECEIVER SPEED PROGRAMMING CONSIDERATIONS

In the DH11, speed code 1110 selects External Input A. In the DH/DM, this speed code selects 19.2K baud. In the DH11, speed code 1111 selects External Input B. In the DH/DM, this speed code selects the output of a clock on the board that can be set for any speed in the range from 150 to 9600 baud. The output of this source is also selected in response to speed code 0110 which in the DH11, selects 200 baud. The DH/DM is shipped with this source set to provide the 200 baud rate. Thus, the user has the option of retaining the 200 baud rate selection in response to the DH11 200 baud speed code or, if this rate is not required, of obtaining a selectable rate in response to the DH11 External B speed code.

In the DH/DM, different non-zero receiver and transmitter speeds can be selected for a given line only if one of these rates is obtained from the source shared by the 200 baud and External P speed codes. If this restriction is not observed, the programmed transmitter speed determines both the transmitter and the receiver speeds for the line.

The zero baud selection provides the means by which the program can turn off any line. A useful application of this capability involves turning off unused line receivers in the presence of excessive circuit noise so as to avoid the receipt of spurious characters.

6.4 BREAK CONTROL TIMING

In order to time the transmission of a break so that no significant message characters are lost, the transmitter interrupt associated with a dummy message containing two null characters is used to time the setting of the BREAK bit for the line.

The use of the dummy message is necessary because the transmitter interrupt indicates the completion of the message transfer from the message buffer in the computer memory to the DH/DM rather than the completion of the message transmission by the DH/DM. This interrupt timing allows the program to write message (n + 1) in the message buffer and write the starting address and word count for this message while the final characters of message n are being transmitted. Specifically, at the time of the transmitter interrupt, there are two message characters still to transmitted, one in the UART transmit holding register. Thus, by using the interrupt associated with the dummy message to time the setting of the BREAK bit, the break is started when the two null characters of this message reside in these registers. (The break begins at the instant that the BREAK bit for the line is set in the break control register.)

A second dummy message can be used to time the duration of the break. This message should be made up of null characters, since the last two characters are actually transmitted after the transmitter interrupt associated with the message has been used to time the resetting of the BREAK bit for the line. This timing method provides a break duration equal to the character period times the number of characters in the second dummy message. (The break ends before the final two characters of the second dummy message are transmitted but it includes the two character periods of the first dummy message transmission.)

6.5 TRANSMITTER AND RECEIVER TIMING CONSIDERATIONS

Because characters are transmitted asynchronously, message integrity is not affected by the speed with which characters are supplied to the UART. Continous transmission is achieved if the UART transmit holding register receives character (n + 1) during the period when character n is being transmitted. Since the DH/DM uses word accesses to PDP-11 memory, only one DMA access is required for every two transmit characters. However, to maintain continous transmission each access must be completed within one character period of its initiation.

The 255-word silo provdes buffer storage for received characters. If the silo becomes full, then characters cannot be transferred to it from UART receiver holding registers. Thus, if this happens, characters may be overwritten in one or more UART modules. The amount of time that the program has to service a receiver interrupt depends upon the number of lines from which messages are currently being received, the receiver speeds, and the silo alarm level value that has been written in the silo

status register. A low silo alarm level value increases the time available to respond to the interrupt. However, if the program responds immediately, the lower value increases program overhead because more interrupts will have to be serviced to transfer a given number of characters. The DH/DM decreases this overhead by interrupting after sixteen characters have been received or after 20ms have passed since the first character is received.

If the transfer of a character from the holding register of a UART receiver has to be inhibited because the silo is full, STORAGE INTERRUPT bit 14 of the system control register is set and if STORAGE INTERRUPT ENABLE bit 12 is set, an interrupt request is initiated to inform the program that the silo is full. The program may still have time to empty the silo before an overrun occurs.

6.6 MAINTENANCE MODE CONSIDERATIONS

When maintenance (bit 9 of the system control register) is set, the UART modules are placed in the local loopback mode. In this mode, the receiver input from the line is ignored, the transmitter output to the line is held at the marking level, and the serial output from each UART transmitter shift register is connected to the serial input of the receiver shift register so that each character transmitted by the transmitter section is received by the receiver section. The silo is reduced to 64 words and the clock is forced to 200 baud.

Also, when MAINTENANCE is set, the PDP-11 program can write the STORAGE INTERRUPT, NON-EXISTENT-MEMORY INTERRUPT, and RECEIVER-INTERRUPT (system control register bits 14, 10, and 07) which are normally read only.

When SILO MAINTENANCE (bit 15 of the silo status register) is set, a 1010101010101010 is loaded into the silo. Each successive clearing and setting of SILO MAINTENANCE loads another copy of this pattern into the silo. In order to fill the silo with this test pattern, all receiver speeds must be set to zero baud and the silo must be emptied of previously received line characters.

When the DH/DM cables are installed in the loopback connectors, the following occur:

- Silo size is reduced to 64 words.
- On-board clock is forced to 200 baud.
- Secondary transmit and secondary receive are internally looped together.
- Clear to Send is the same as Carrier.
- Ring and Request to Send are internally looped together.

BLANK

SECTION 7

How DH/DM Works

The DH/DM is a microprocessor-based device which emulates two DEC devices, the DH11 and the DM11-BB. The basic DH emulation provides an interface between a standard Unibus and sixteen asynchronous communications lines. The DM emulation provides sufficient modem control to allow the DH/DM to interface with the most commonly used data sets as well as with local devices.

The purpose of this section is to afford some insight into how the DH/DM works rather than to describe the specifics of the emulation. However, certain features of the emulation provide enhancements of the emulated devices and these features are described. There are also certain limitations of the emulation that have been accepted in order to achieve the objective of a single hex board device. Although these limitations are not significant for most applications, they are also described.

The sixteen lines serviced by the DH/DM time-share many facilities that would have to be duplicated in separate interfaces. The consequent cost reductions make practical the use of additional performance-enhancing features. The multiplexing of the sixteen lines also minimizes the peripheral address space allocation and Unibus loading associated with servicing the lines.

DH/DM message handling techniques are most advantageous in an interactive environment. In such an environment, outgoing computer messages tend to be longer than incoming messages from the interactive terminals. The DH/DM minimizes computer program participation in message transmission by using direct memory access (DMA) to obtain transmit message characters from data buffers in computer memory. For incoming messages from terminals, computer memory space allocation is minimized and computer responsiveness is maximized by using another technique. Message characters from all lines are tagged and queued in the DH/DM first-in first-out (FIFO) buffer for handling by a computer program routine called in response to a receiver interrupt from the DH/DM.

The DH/DM allows the computer program to select the character format and transmit and receive speeds for each line. This allows the format and speed requirements of various terminals to be met and the differing speeds of various data sets to be utilized without using configuration procedures such as jumper placement modification.

7.1 MESSAGE TRANSMISSION

The computer program places a message to be transmitted over a particular line in a data buffer (set of consecutive locations) in computer memory. The data buffer performs the following tasks:

- Writes the line number into the system control register
- Writes the starting address of the data buffer into the current address register
- Writes the complement of the number of message characters into the byte count register
- Sets the bit associated with the line in the buffer active register

The DH/DM now initiates the non-processor requests required to obtain the message characters from memory and transmits them without further intervention from the program. After the final message character has been obtained from memory, the DH/DM resets the bit associated with the line in the buffer active register. If enabled, this causes the initiation of a transmitter interrupt to inform the program that the data buffer has been emptied. This also implies that after two more character periods, the message transmission will have been completed.

To maximize the efficiency of the Unibus, the DH/DM generally uses word accesses, rather than byte accesses. However, this does not impose any limitations on data buffer locations or lengths since the DH/DM is capable of performing byte accesses when required.

The conversion of each parallel character to a serial asynchronous character is performed by the transmitter section of a Universal Asynchronous Receiver Transmitter (UART) module. The serial character format and baud rate are determined by information written by the program into the line parameter register. The UART contains a transmit holding register which provides buffer storage for one character and a transmit shift register which performs the parallel to serial conversion. When the bit for a particular line in the buffer active register is set, the DH/DM functions to obtain the next character for a line and loads that character into the UART transmit holding register for the line each time the transmit holding register becomes available. When the final character of the message is loaded into the transmit holding register, the buffer active register bit for the line is reset.

A maximum of two character periods are required to complete the transmission of the character now in the transmit shift register and the character which is loaded into the transmit holding register.

7.2 MESSAGE RECEPTION

Each serial asynchronous character that is received from a communication line is converted to parallel form by the receiver section of a UART module associated with that line. The receiver section contains a receive shift register which performs the serial-to-parallel conversion and a receive holding register which provides buffer storage for a character. The receiver section verifies that each character is framed by the specified stop bit(s). If parity generation/checking is specified by the line parameter register information for that line, it also verifies that the received character exhibits the specified parity.

As characters become available in the receive holding registers, they are tagged with their line numbers, with a data present bit, and with error flags from the UART receiver. They are also queued in a silo for subsequent transfer to the computer under program control. The silo is a first-in, first-out memory whose output end is the next received character register which is read by the computer program. Words loaded into the top of the silo automatically propagate toward the bottom as locations become available. As each word is read out of the next received character register, that register becomes available to read the next word which automatically propagates into it.

A receiver interrupt is initiated to inform the program that the silo should be emptied. If enabled, this interrupt is initiated when the number of words in the silo exceeds the silo alarm level specified in the silo status register. Opposing considerations affect the setting of the silo alarm level. Efficiency is proportional to the number of words handled during each servicing sequence because entry and exit overhead is averaged over more character processing operations. However, under heavy traffic conditions, an increase in the silo alarm level increases the possibility of a silo overflow. Under light traffic conditions, the problem of response time to short messages arises. There are two conventional solutions to the response time problem. One of these is to set the silo alarm level at zero so that one single character message is serviced. The other is to use both the receiver interrupt and a real time clock interrupt to call the silo servicing routine. The call from the real time clock interrupt establishes the maximum response delay under light traffic conditions. The DH/DM receiver interrupt implementation contains a special feature which enhances the first of these solutions. The DH/DM delays the receiver interrupt for 20 milliseconds after the specified silo alarm level has been exceeded, unless the silo fill level reaches 16 during that delay time, in which case it immediately initiates the interrupt. This improves silo servicing efficiency while ensuring the servicing of single-character messages under light traffic conditions without the need for a spearate real time clock interrupt.

The DH/DM silo has a capacity of 255 words, rather than the conventional 64. This decreases the possibility of silo overflow under heavy traffic conditions.

Because the DH/DM uses random-access memory (RAM) and pointers to implement the silo, the propagation delay associated with FIFO buffer memories is not encountered. This provides an increase in efficiency because any word which enters the silo while it is being emptied is immediately ready for transfer during that pass through the silo servicing routine.

7.3 MODEM CONTROL

In order to transmit data between the computer and remote terminals, data sets (modems) are used to perform the conversions between the serial data signals supplied and accepted by the computer and terminals and the signals suitable for transmission over telephone lines. In addition to the main transmit and receive data signals passing between the data sets and the interfacing equipment, a variety of control signals and, in some cases, secondary data signals, may be required, in accordance with the particular data sets being used. EIA standard RS232C defines sixteen control signals; however, most data sets require only a small subset of these signals.

For each line, the DH/DM monitors two data set output control signals, RING and CARRIER, and controls one data set input control signal, DATA TERMINAL READY. This allows communication over switched or dedicated telephone lines using Bell Model 103 type full duplex modems.

The DH/DM scans the RING and CARRIER signals from the sixteen lines looking for a change of state on any of these lines. When it detects a change of state, it stops scanning, holds the line number where the change has been detected and if enabled, initiates a DM interrupt request to the computer. By reading the DM control and status register of the DH/DM, the program can then determine the line associated with the interrupt and the control signal that has changed state.

When operating over switched telephone lines, the data set asserts the RING signal in response to each ring received on the incoming communication line. In response to the RING signal assertion, the program asserts the DATA TERMINAL READY signal for the line. This is analogous to removing the telephone from its hook and saying hello. It thus allows the connection to be maintained. If data is received from the opposite end of the link, the data set asserts the CARRIER signal. The assertion of CARRIER informs the program that the connection should be maintained (by continuing to assert DATA TERMINAL READY) to allow the reception of a message. At the end of the message, the assertion of CARRIER is terminated. When this is detected, the connection is then dropped by the program which terminates the assertion of DATA TERMINAL READY.

The modem control portion of the DH/DM is designed to provide the modem control supported by most of the operating systems used in the interactive environments in which the DH/DM is typically used. The DH/DM provides the same modem control as the DZ11. In applications requiring full modem control, an ABLE DMAX/16 with a DM/16 dataset control board option can be used.

7.4 SPECIAL APPLICATION OF RING SIGNAL

In applications where modem control is not required, the RING line can be used as a device handshake signal which stops transmissions to that device in a manner that is completely transparent to the software. This is particularly advantageous for a device which can accept bursts of data at a high speed but cannot accept data when certain time consuming tasks are being implemented.

For this application, a jumper placement on the DH/DM circuit board connects the RING line to the clear-to-send input of the UART associated with the line. (Without this jumper placement, the clear-to-send is held continuously at the active level.) When so configured, the UART clear-to-send input is removed when the RING signal is placed at the inactive level. The loss of clear-to-send inhibits the UART from raising its transmitter-ready flag and thus the next character is not loaded into the transmit holding register until the clear-to-send signal has been restored by reactivation of the RING signal.

7.5 BAUD RATE SELECTION

The DH/DM includes an on-board programmable baud rate generator which can be used to provide essentially any required baud rate over the range from 150 baud to 10.25K baud. One limitation on the use of this generator is that it is the only available source of 200 baud, one of the standard DH11 baud rates.

Special applications that require different speeds for receive and transmit (split baud rates) are handled differently from the DH11. The internal baud rate selector of each USART is used to set the speed of either the receiver or the transmitter in the usual manner. The other speed is obtained by selecting the appropriate speed for the clock and programming External B (1111) or 200 baud (0110) into the Line Parameter Register.

7.6 DH/DM DIAGNOSTIC MICROPROGRAM

In order to eliminate the need for running software diagnostic programs to verify DH/DM operation and to facilitate troubleshooting of the DH/DM, the DH/DM contains a resident diagnostic microprogram. This is divided into seven sections, five of these sections comprise an internal self-test which can be executed without any substantial investment of time and without utilization of any facilities external to the DH/DM. Three program switches are used to specify the utilization of the diagnostic microprogram. When these switches are set for normal DH/DM operation, the five sections comprising the internal self test normally execute when power is applied to the DH/DM. If each section is successfully completed, control is passed to the operational program. If a test fails, the diagnostic microprogram retains control and one or more diagnostic LED indicators remain lit, providing information about the type of fault that has been detected. The successful completion of these five diagnostic microprogram sections verifies about 75% of the DH/DM circuitry.

The two sections of the diagnostic microprogram which do not execute as part of the basic self test, are the UART test and the bus test. The UART test section is omitted because it requires a substantial amount of time to run. The bus test section is omitted because it utilizes facilities external to the DH/DM. When the program switches are positioned so these sections also execute, essentially 100% of the DH/DM is exercised.

In addition to determining what sections are executed, the program switches provide the means of selecting various procedures to be followed when a fault is detected or looping through a section in which a fault is detected. A mode in which DH/DM loops continuously through the entire diagnostic microprogram can also be selected.

Appendix A
Priority Strapping

This appendix contains a wiring table and diagram for priority interrupt levels on the DH/DM. The DH/DM is factory set to level BR5 for the DH and level BR4 for the DM. These are the correct interrupt levels for most users. If you require different priorities, use the table and diagram in this appendix to strap new priority levels.

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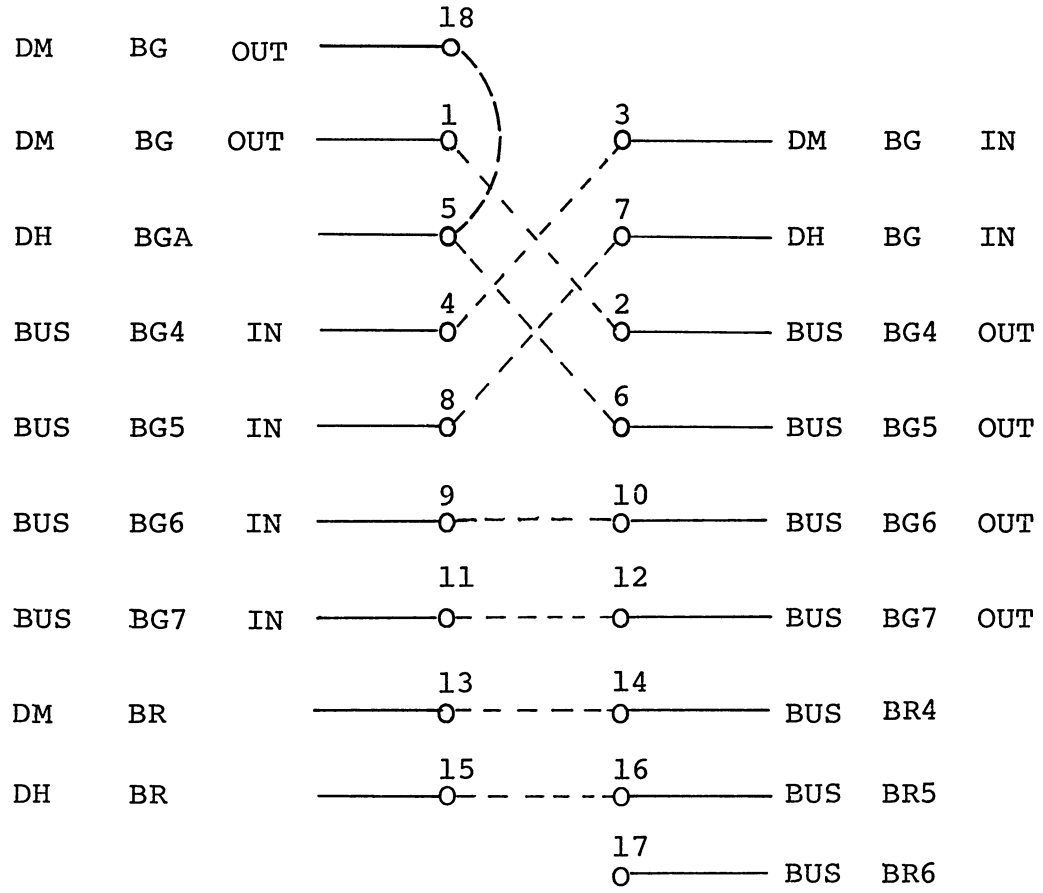
DH LEVEL	DM LEVEL	'E' POINT JUMPER CONNECTIONS																	
		FROM	TO	FROM	TO	FROM	TO	FROM	TO	FROM	TO	FROM	TO	FROM	TO	FROM	TO	FROM	TO
4	4	E4	E7	E5	E3	E1	E2	E15	E14	E13	E14	E8	E6	E9	E10	E11	E12		
4	5	E4	E7	E5	E2	E1	E6	E15	E14	E13	E16	E3	E8	E18	E5	E11	E12	E9	E10
4	6	E4	E7	E5	E2	E1	E10	E15	E14	E13	E17	E3	E9	E18	E5	E11	E12	E6	E8
5	4	E8	E7	E5	E6	E1	E2	E15	E16	E13	E14	E3	E4	E18	E5	E11	E12	E9	E10
5	5	E8	E7	E5	E3	E1	E6	E15	E16	E13	E16	E4	E2	E9	E10	E11	E12		
5	6	E8	E7	E5	E6	E1	E10	E15	E16	E13	E17	E3	E9	E18	E5	E11	E12	E4	E2
6	4	E9	E7	E5	E10	E1	E2	E15	E17	E13	E14	E3	E4	E18	E5	E11	E12	E6	E8
6	5	E9	E7	E5	E10	E1	E6	E15	E17	E13	E16	E3	E8	E18	E5	E11	E12	E4	E2
6	6	E9	E7	E5	E3	E1	E10	E15	E17	E13	E17	E8	E6	E4	E2	E11	E12		

DH/DM Priority Strapping Chart



- - - - -: Indicates Factory Wired

OPTIONAL INTERRUPT LEVEL STRAPPING

(Use only if you wish to use Priority Interrupt Levels that differ from standard DEC levels.)

Appendix B
List of Materials

This appendix contains lists of materials for the DH/DM board including vendors and parts numbers.

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Description	Vendor Part No.	ACT Part No.	Qty.	Reference Designation	Vendor
PWB-16 CH Async. DMA Com Cntrlr.		10103001	1		
ART-16 CH Async. DMA Com Cntrlr.		10103002	Ref.		
Schem-16 CH Async. DMA Com Cntrlr.		10103003	Ref.		
Resistor 5% ¼W 1K	RC07GF102J	310-012-102	6	R1,2,3,10,11,15	
Resistor 5% ¼W 220	RC07GF221J	310-012-221	1	R5	
Resistor 5% ¼W 33K	RC07GF333J	310-012-333	6	R4,6,7,8,12,13	
Resistor 5% ¼W 4.7K	RC07GF472J	310-012-472	4	R9,14,16,17	
Resistor Module,8 Pin,Sip,5%,180	MSP08A01-181J	311-181-002	1	RM9	Dale
Resistor Module,8 Pin,Sip,5%,470	MSP08A01-471J	311-471-002	2	RM1,6	Dale
Resistor Module,8 Pin,Sip,5%,1K	MSP08A01-102J	311-102-002	2	RM15,25	Dale
Resistor Module,8 Pin,Sip,5%,33K	MSP08A01-333J	311-333-004	6	RM5,7,10,16,22,23	Dale
Resistor Module,8 Pin,Sip,5%,4.7K	MSP08A01-472J	311-472-002	8	RM2,3,4,14,18,19, 24,28	Dale
Resistor Module,8 Pin,Sip,5%,4.7K	MSP08A03-472J	311-472-003	8	RM11,12,13,17,20, 21,26,27	Dale
Resistor Module,8 Pin,Sip,5%,180/ 390	764-5-R180/ 390	312-121-002	1	RM8	Beckman
Capacitor,Silver Mica,5%,HV,200 PF	CD15FD201J03	320-029-201	1	C40	Cornell
Capacitor,Silver Mica,5%,HV,47 DPF	CD15FD471J03	320-029-471	2	C41,46	Cornell
Capacitor,Ceramic,AXIAL,10%, 50V, .01MF	CK12BX103K	322-226-103	35	C7-39,42,43	Corning
Capacitor,Tantalum 20%,20V, 4.7MF	CCM-020-475-20	322-244-475	8	C1-6,44,45	Corning
Capacitor Module, 8 Pin,Sip, 470PF	460CH471X9PD	321-637-471	2	CM1,2	Sprauge
Optcis LED Quad	555-4003	331-204-001	1	CR1	Dialight
Diode Zener 3.3V 1W	1N4728A	341-303-302	2	CR2,3	Fairchild
I.C. Interface Quad Driver	1488	345-001-488	8	U88,95,101,108,114, 122,126,134	Motorola
I.C. Interface Quad Receiver	1489	345-001-489	12	U58,64,76,77,82,83, 98,111,121,125,133,137	Motorola
I.C. Interface Quad Receiver O.C.	8640	345-008-640	1	U74	Nat'l.
I.C. Interface Quad Bus Xceiver O.C.	8641	345-008-641	3	U9,63,68	Nat'l.
I.C. Interface Quad Bus Xceiver W/Logic	2908	345-029-008	10	U32,33,39,45,51,81, 87,94,97,120	AMD
I.C. Interface Octal Invtr/Line Drvr 3 St.	74LS240	345-274-240	7	U52,70,100,110,112, 124,132	T.I.

AMD = Advanced Micro Devices, T.I. = Texas Instruments

Table C-1: List of Materials

Description	Vendor Part No.	ACT Part No.	Qty.	Reference Designation	Vendor
I.C. Interface Octal Buff./Line Drvr. 3 St.	74LS244	345-274-244	1	U18	T.I.
I.C. Ram 64x4 O.C.	74S189	347-174-189	2	U24,28	T.I.
I.C. Ram 4K 1024x4 Tri-St.	2148	347-421-480	2	U34,40	Intel
I.C. Hex Inverter	7404	349-074-004	1	U80	T.I.
I.C. Quad 2 In NAND Buffer O.C.	7438	349-074-038	2	U69,75	T.I.
I.C. 8 to 3 Priority Encoder	74148	349-074-148	1	U48	T.I.
I.C. Quad 2 In NAND	74S00	349-174-000	3	U62,71,73	T.I.
I.C. Hex Inverter	74S04	349-174-004	2	U60,67	T.I.
I.C. Quad 2 In AND	74S08	349-174-008	2	U43,78	T.I.
I.C. Triple 3 In NAND	74S10	349-174-010	2	U49,55	T.I.
I.C. Triple 3 In AND	74S11	349-174-011	1	U61	T.I.
I.C. Quad 2 In OR	74S32	349-174-032	1	U29	T.I.
I.C. Dual D Flip Flop	74S74	349-174-074	2	U93,96	T.I.
I.C. Quad 2 In XOR	74S86	349-174-086	1	U65	T.I.
I.C. Dual J-K Flip Flop	74S112	349-174-112	1	U109	T.I.
I.C. 13 Input NAND	74S133	349-174-133	1	U57	T.I.
I.C. 3 to 8 Decoder	74S138	349-174-138	3	U26,31,106	T.I.
I.C. Dual 2 to 4 Decoder	74S139	349-174-139	2	U37,59	T.I.
I.C. 3 to 8 Decoder	74ES138	349-274-138	2	U84,85	T.I.
I.C. 8 to 1 Mux	74S151	349-174-151	1	U30	T.I.
I.C. Quad 2 to 1 Mux	74S157	349-174-157	2	U25,46	T.I.
I.C. Hex D Flip Flop	74S174	349-174-174	1	U42	T.I.
I.C. Quad 2 to 1 Mux	74LS157	349-274-157	2	U20,21	T.I.
I.C. Microprocessor	2901B	349-229-001	2	U22,23	AMD
I.C. Microprogram Sequencer	2911	349-229-011	3	U1,12,13	AMD
I.C. Dual D Flip Flop	74LS74	349-274-074	1	U72	T.I.
I.C. 8 Bit Addressable Latch	74LS259	349-274-259	2	U47,53	T.I.
I.C. 8 Bit Latch Tri-St.	74LS373	349-274-373	1	U79	T.I.
I.C. Octal D Flip Flop Tri-St.	74LS374	349-274-374	8	U10,11,14,15,17,19, 119,123	T.I.
I.C. Octal D Flip Flop W/Enable	74LS377	349-274-377	5	U35,36,66,86,131	T.I.
I.C. 4 Bit Sync Counter	74LS161	349-274-161	2	U135,138	Signetics
I.C. Usart	2651	349-402-651	16	U89-92,102-105,115-118, 127-130	
I.C. 8 to 1 Mux	74LS151	349-274-151	1	U16	
I.C. 8 Bit Comparator	25LS2521	349-252-521	2	U38,44	AMD

T.I. = Texas Instruments, AMD = Advanced Micro Devices

Table C-2: List of Materials

Description	Vendor Part No.	ACT Part No.	Qty.	Reference Designation	Vendor
Oscillator, 10.1376Mhz	K1114A	391-013-771	1	U99	Motorola
Socket Pin PC Mount	LSG-1AG2-1	570-400-101	4	(U99)	Augat
Switch 8 Pos Dip	76SB08	412-081-101	4	S1,2,5,6	Grayhill
Switch 10 Pos Dip	76SB10	412-101-101	2	S3,4	Grayhill
Wire Wrap Post	P025-443-1	560-400-101	61	E1-61	S. Phillips
Connector, Flat Cable, Rt. Ang., 40 Pin	3495-1002	564-404-005	1	J3	3 M
Conn., Flat Cbl., Rt. Ang., 50 Pin, Lock	3433-1302	564-405-003	2	J1,2	3 M
Socket IC 20 Pin	520-AG-11D	575-402-001	2	(U27,54)	Augat
Socket IC 24 Pin	524-AG-11D	575-402-401	7	(U2-4,6-8,41)	Augat
Handle PC Extractor, Left	111-10-1	630-100-004	1		Calmark
Handle PC Extractor, Right	111-10-2	630-100-005	1		Calmark

Table C-3: List of Materials

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Appendix C
Spare Parts List

This appendix provides recommended spare parts lists for the DH/DM board, for those wishing to maintain a parts inventroy.

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Part	ACT Part	Vendor Part No.	Vendor	Reference Designation
I.C. Interface Quad Driver	345-001-488	1488	Motorola	U88,95,101,108, 114,122,126,134
I.C. Interface Quad Receiver	345-001-489	1489	Motorola	U58,64,76,77, 82,83,98,111, 121,125,133,137
I.C. Interface Quad Receiver O.C.	345-008-640	8640	National	U 74
I.C. Interface Quad Bus Xceiver O.C.	345-008-641	8641	National	U 9,63,68
I.C. Interface Quad Bus Xceiver W/Logic	345-029-008	2908	AMD	U32,33,39,45,51, 81,87,94,97,120
I.C. Interface Octal Invtr/Line Drvr. 3 St.	345-274-240	74LS240	T.I.	U52,70,100,110, 112,124,132
I.C. Interface Octal Buff./ Line Drvr. 3 St.	345-274-244	74LS244	T.I.	U18
I.C. Ram 64x4 O.C.	347-174-189	74S189	T.I.	U24,28
I.C. Ram 4K 1024x4 Tri-St.	347-421-480	2148	Intel	U34,40
I.C. Hex Inverter	349-074-004	7404	T.I.	U80
I.C. Quad 2 In NAND Buff.O.C.	349-074-038	7438	T.I.	U69,75
I.C. 8 to 3 Priority Encoder	349-074-148	74148	T.I.	U48
I.C. Quad 2 In NAND	349-174-000	74S00	T.I.	U62,71,73
I.C. Hex Inverter	349-174-004	74S04	T.I.	U60,67
I.C. Quad 2 In AND	349-174-008	74S08	T.I.	U43,78
I.C. Triple 3 In NAND	349-174-010	74S10	T.I.	U49,55
I.C. Triple 3 In AND	349-174-001	74S11	T.I.	U61
I.C. Quad 2 In OR	349-174-032	74S32	T.I.	U29
I.C. Dual D Flip Flop	349-174-074	74S74	T.I.	U93,96
I.C. Quad 2 In XOR	349-174-086	74S86	T.I.	U65
I.C. Dual J-K Flip Flop	349-174-112	74S112	T.I.	U109
I.C. 13 Input NAND	349-174-133	74S133	T.I.	U57
I.C. 3 to 8 Decoder	349-174-138	74S138	T.I.	U26,31,106
I.C. Dual 2 to 4 Decoder	349-174-139	74S139	T.I.	U37,59
I.C. 3 to 8 Decoder	349-274-138	74LS138	T.I.	U84,85
I.C. 8 to 1 Mux	349-174-151	74S151	T.I.	U30
I.C. Quad 2 to 1 Mux	349-174-157	74S157	T.I.	U25,46
I.C. Hex D Flip Flop	349-174-174	74S174	T.I.	U42
I.C. Quad 2 to 1 Mux	349-274-157	74LS157	T.I.	U20,21
I.C. Microprocessor	349-229-001	2901B	AMD	U22,23
I.C. Microprogram Sequencer	349-229-011	2911	AMD	U1,12,13
I.C. Dual D Flip Flop	349-274-074	74LS74	T.I.	U72
I.C. 8 Bit Addressable Latch	349-274-259	74LS259	T.I.	U47,53
I.C. 8 Bit Latch Tri-St.	349-274-373	74LS373	T.I.	U79
I.C. Octal D Flip Flop Tri-St.	349-274-374	74LS374	T.I.	U10,11,14,15, 17,19,119,123
I.C. Octal D Flip Flop W/Enable	349-274-377	74LS377	T.I.	U35,36,66,86,131
I.C. 4 Bit Sync Counter	349-274-161	74LS161	T.I.	U135,138

T.I. = Texas Instruments, AMD = Advanced Micro Devices

Spare Parts List

Part	ACT Part	Vendor Part No.	Vendor	Reference Designation
I.C. Usart	349-402-651	2651	Signetics	U89-92,102-105, 115-118,127-130
I.C. 8 to 1 Mux	349-274-151	74LS151		U16
I.C. 8 Bit Comparator	349-252-521	25LS2521	AMD	U38,44
AMD = Advanced Micro Devices				

Table A-1(Con't.): Spare Parts List

Appendix D

Address Switch Settings For VAX/VMS Systems

This appendix provides address switch setting charts necessary for installing DH/DM in VAX/VMS systems.

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ADDRESS SWITCH SETTINGS FOR VAX/VMS SYSTEMS

UNIT	DH START ADDRESS	DM START ADDRESS	DH VECTOR	DM VECTOR
1	763740	763760	740	750
2	763700	763720	720	730
3	763640	763660	700	710
4	763600	763620	660	670
5	763540	763560	640	650
6	763500	763520	620	630
7	763440	763460	600	610
8	763400	763420	560	570
9	763340	763360	540	550
10	763300	763320	520	530
11	763240	763260	500	510
12	763200	763220	460	470
13	763140	763160	440	450
14	763100	763120	420	430
15	763040	763060	400	410
16	763000	763020	360	370

UNIT	ADDRESS SWITCH 2 POSITION 8 7 6 5 4 3 2 1	ADDRESS SWITCH 5 POSITION 8 7 6 5 4 3	ADDRESS SWITCH 6 POSITION 8 7 6 5 4 3 2
1	- - - - - - - C	C C C C - -	C C C C - C -
2	- - - - - - C - C	C C C - C -	C C C - C C -
3	- - - - C - - C	C C C - - -	C C C - - C -
4	- - - - C C - C	C C - C C -	C C - C C C -
5	- - - C - - - C	C C - C - -	C C - C - C -
6	- - - C - C - C	C C - - C -	C C - - C C -
7	- - - C C - - C	C C - - - -	C C - - - C -
8	- - - C C C - C	C - C C C -	C - C C C C -
9	- - C - - - - C	C - C C - -	C - C C - C -
10	- - C - - C - C	C - C - C -	C - C - C C -
11	- - C - C - - C	C - C - - -	C - C - - C -
12	- - C - C C - C	C - - C C -	C - - C C C -
13	- - C C - - - C	C - - C - -	C - - C - C -
14	- - C C - C - C	C - - - C -	C - - - C C -
15	- - C C C - - C	C - - - - -	C - - - - C -
16	- - C C C C - C	- C C C C -	- C C C C C -

S1-1 Open
S1-7 DM Enabled: Open; DM Disabled: Closed
S1-8 Open
S2-1 Closed
S2-2 DM Enabled: Open; DM Disabled: Closed

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